深圳市金逸晨电子有限公司

ShenZhen GoldenMorning Electronic CO.,LTD

PRODUCT SPECIFICATION FOR OLED MODULE

Revision: V1.0

Model No:

GME12864-49	GME12864-52
GME12864-50	GME12864-53
GME12864-51	GME12864-54

APPROVED SIGNATURE

□ Approved Product Specification only

■ Approved Product Specification and Samples

Prepared By	Checked By	Approved By

GENERAL SPECIFICATION

MODULE NO. :

CUSTOMER P/N:

VERSION NO.	CHANGE DESCRIPTION	DATE
1.0	ORIGINALVERSION	2020/04/22

CONTENTS

1. FUNCTIONS & FEATURES

- LCD TYPE:

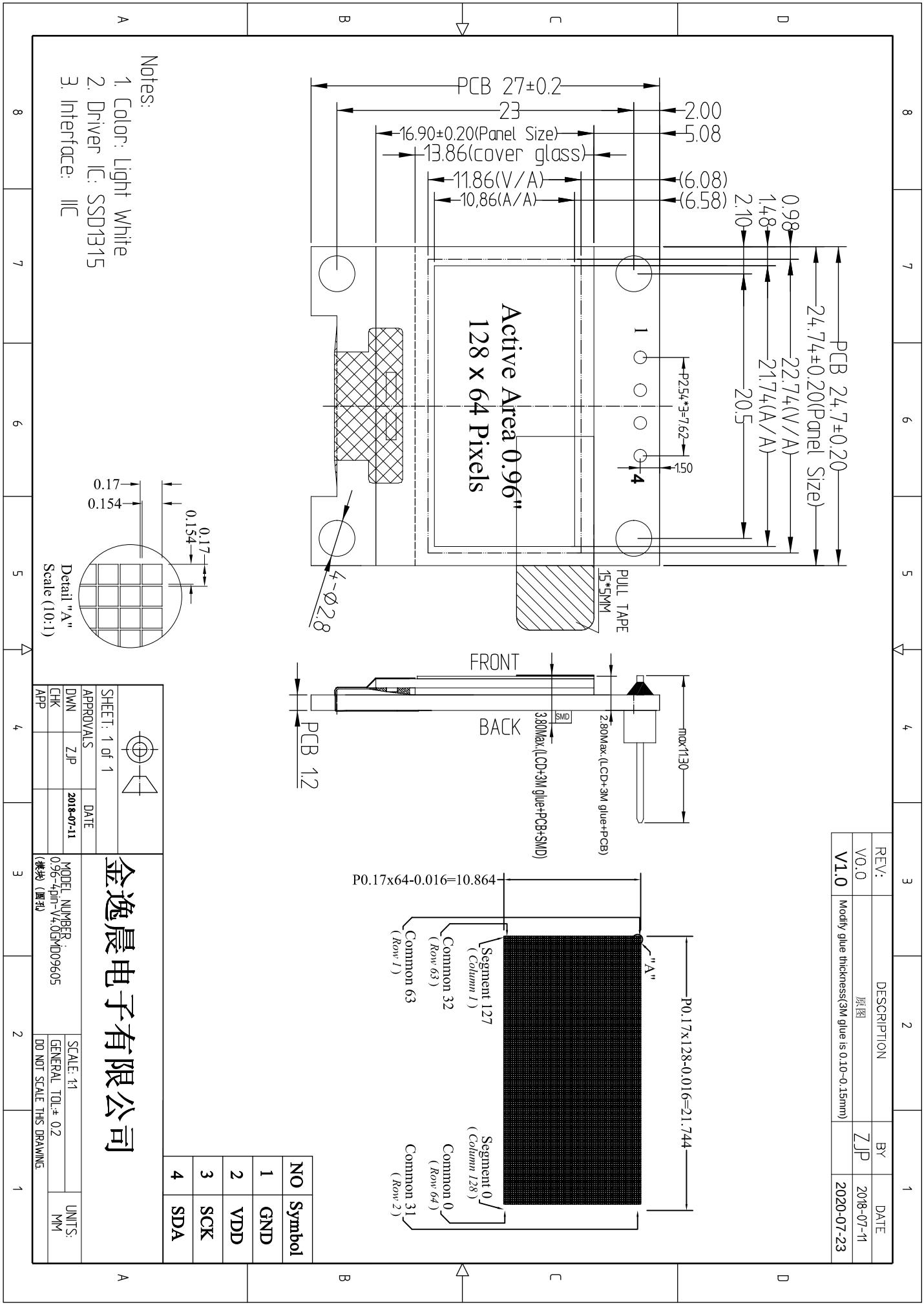
MODULE MODEL	LCD TYPE	REMARK
2864KLWEG01	0.96" OLED Passive Matrix	

- Driving Scheme : 1/64 Duty,
- Viewing direction : 6 O'clock
- Drive IC : SSD1315
- Power Supply Voltage : 3.0V
- V_{CC} : 12.0V
- Interface : IIC
- RoHS Compliant

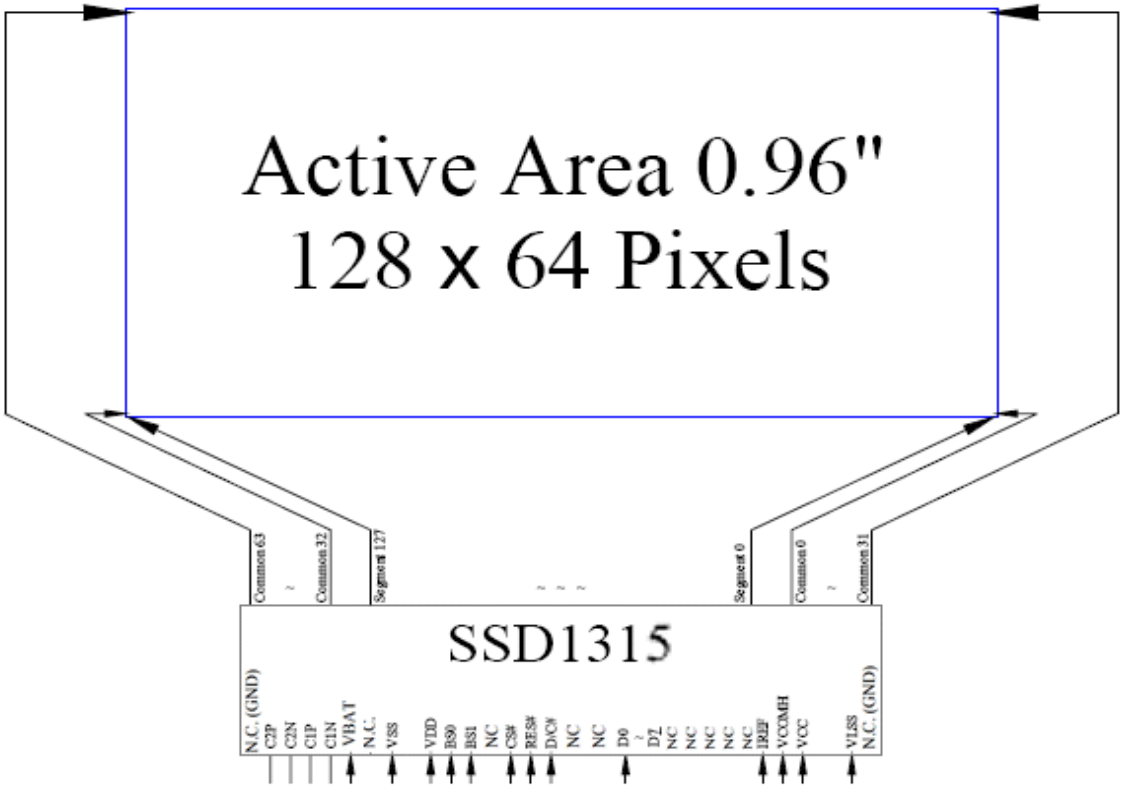
2. MECHANICAL SPECIFICATIONS

- Module Size : 24.7(L)X27(W)X11.3Max(T)mm
- Viewing Area : 22.74(L) x 11.86 (W) mm
- Active Area : 21.74 (L) x 10.86 (W) mm
- Dot Pitch : 0.154 (W) x 0.154 (H) mm
- Dot Size : 0.17(W) x 0.17(H) mm

3. EXTERNAL DIMENSIONS (unit: mm)



4. BLOCK DIAGRAM



5. PIN ASSIGNMENT

PIN	SYMBOL	Descriptions
1	GND	Ground of Logic Circuit
2	VDD	Power Supply for Logic
3	SCK	Serial clock input.
4	SDA	Serial data input.

6. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for Logic	V_{DD}	-0.3	4	V	1, 2
Supply Voltage for Display	V_{CC}	0	16	V	1, 2
Supply Voltage for DC/DC	*V_{BAT}*	*-0.3*	*5*	*V*	*1, 2*
Operating Temperature	T_{OP}	-40	85	°C	
Storage Temperature	T_{STG}	-40	85	°C	3
Life Time (120 cd/m^2)		10,000	-	hour	4
Life Time (80 cd/m^2)		30,000	-	hour	4
Life Time (60 cd/m^2)		50,000	-	hour	4

Note 1: All the above voltages are on the basis of "V_{SS} = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. "Optics & Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

Note 3: The defined temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80°C.

Note 4: V_{CC} = 12.0V, T_a = 25°C, 50% Checkerboard.
Software configuration follows Section 4.4 Initialization.
End of lifetime is specified as 50% of initial brightness reached. The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

7. ELECTRICAL CHARACTERISTICS

7.1. Optics Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Brightness (V_{CC} Supplied Externally)	L_{br}	Note 5	80	100	-	cd/m^2
Brightness (V_{CC} Generated by Internal DC/DC)	*L_{br}*	*Note 6*	*50*	*60*	*-*	*cd/m^2*
C.I.E. (Blue)	(x) (y)	C.I.E. 1931	0.10 0.20	0.14 0.24	0.18 0.28	
C.I.E. (Yellow)	(x) (y)	C.I.E. 1931	0.43 0.45	0.47 0.49	0.51 0.53	
Dark Room Contrast	CR		-	2000:1	-	
Viewing Angle			-	Free	-	degree

* Optical measurement taken at V_{DD} = 2.8V, V_{CC} = 12V & *7.25V*.
Software configuration follows Section 4.4 Initialization.

7.2. DC CHARACTERISTICS

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage for Logic	V_{DD}		1.65	2.8	3.3	V
Supply Voltage for Display (Supplied Externally)	V_{CC}	Note 5 (Internal DC/DC Disable)	11.5	12.0	12.5	V
Supply Voltage for DC/DC	*V_{BAT}*	*Internal DC/DC Enable*	*3.5*	*-*	*4.2*	*V*
Supply Voltage for Display (Generated by Internal DC/DC)	*V_{CC}*	*Note 6 (Internal DC/DC Enable)*	*7.0*	*-*	*7.5*	*V*
High Level Input	V_{IH}	I_{OUT} = 100μA, 3.3MHz	0.8×V_{DD}	-	V_{DD}	V
Low Level Input	V_{IL}	I_{OUT} = 100μA, 3.3MHz	0	-	0.2×V_{DD}	V
High Level Output	V_{OH}	I_{OUT} = 100μA, 3.3MHz	0.9×V_{DD}	-	V_{DD}	V
Low Level Output	V_{OL}	I_{OUT} = 100μA, 3.3MHz	0	-	0.1×V_{DD}	V
Operating Current for V_{DD}	I_{DD}		-	180	300	μA
Operating Current for V_{CC} (V_{CC} Supplied Externally)	I_{CC}	Note 7	-	12.3	16	mA
Operating Current for V_{BAT} (V_{CC} Generated by Internal DC/DC)	*I_{BAT}*	*Note 8*	*-*	*21*	*28.0*	*mA*
Sleep Mode Current for V_{DD}	$I_{DD, SLEEP}$		-	1	5	μA
Sleep Mode Current for V_{CC}	$I_{CC, SLEEP}$		-	2	10	μA

Note 5 & *6*: Brightness (L_{br}) and Supply Voltage for Display (V_{CC}) are subject to the change of the panel characteristics and the customer's request.

Note 7: V_{DD} = 2.8V, V_{CC} = 12V, 100% Display Area Turn on.

Note 8: V_{DD} = 2.8V, V_{CC} = 7.25V, 100% Display Area Turn on.

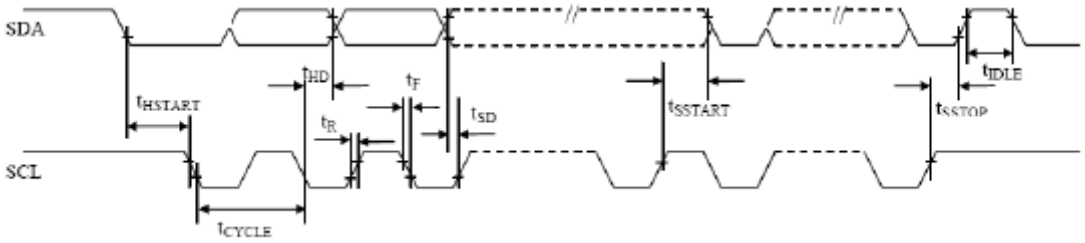
* Software configuration follows Section 4.4 Initialization.

7.3.AC CHARACTERISTICS

1 I^2C Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	µs
t_{HSTART}	Start Condition Hold Time	0.6	-	µs
t_{HD}	Data Hold Time (for "SDA_{OUT}" Pin)	0	-	ns
	Data Hold Time (for "SDA_{IN}" Pin)	300		
t_{SD}	Data Setup Time	100	-	ns
t_{SSTART}	Start Condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	µs
t_{SSTOP}	Stop Condition Setup Time	0.6	-	µs
t_R	Rise Time for Data and Clock Pin		300	ns
t_F	Fall Time for Data and Clock Pin		300	ns
t_{IDLE}	Idle Time before a New Transmission can Start	1.3	-	µs

* (V_{DD} - V_{SS} = 1.65V to 3.3V, T_a = 25°C)



8. COMMANDS SSD1315 Rev 1.0

Fundamental Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	00~0F	0	0	0	0	X_3	X_2	X_1	X_0	Set Lower Column Start Address for Page Addressing Mode	Set the lower nibble of the column start address register for Page Addressing Mode using X[3:0] as data bits. The initial display line register is reset to 0000b after RESET. **Note** (1) This command is only for page addressing mode
0	10~17	0	0	0	1	0	X_2	X_1	X_0	Set Higher Column Start Address for Page Addressing Mode	Set the higher nibble of the column start address register for Page Addressing Mode using X[2:0] as data bits. The initial display line register is reset to 0000b after RESET. **Note** (1) This command is only for page addressing mode
0 0	20 A[1:0]	0 0	0 0	1 0	0 0	0 0	0 0	0 A_1	0 A_0	Set Memory Addressing Mode	A[1:0] = 00b, Horizontal Addressing Mode A[1:0] = 01b, Vertical Addressing Mode A[1:0] = 10b, Page Addressing Mode (RESET) A[1:0] = 11b, Invalid
0 0 0	21 A[6:0] B[6:0]	0 * *	0 A_6 B_6	1 A_5 B_5	0 A_4 B_4	0 A_3 B_3	0 A_2 B_2	0 A_1 B_1	1 A_0 B_0	Set Column Address	Setup column start and end address A[6:0] : Column start address, range : 0-127d, (RESET=0d) B[6:0]: Column end address, range : 0-127d, (RESET =127d) **Note** (1) This command is only for horizontal or vertical addressing mode.
0 0 0	22 A[2:0] B[2:0]	0 0 0	0 0 0	1 0 0	0 0 0	0 0 0	0 A_2 B_2	1 A_1 B_1	0 A_0 B_0	Set Page Address	Setup page start and end address A[2:0] : Page start Address, range : 0-7d, (RESET = 0d) B[2:0] : Page end Address, range : 0-7d, (RESET = 7d) **Note** (1) This command is only for horizontal or vertical addressing mode.
0	40~7F	0	1	X_5	X_4	X_3	X_2	X_1	X_0	Set Display Start Line	Set display RAM display start line register from 0-63 using X_5 $X_4X_3X_2X_1X_0$. Display start line register is reset to 000000b during RESET.

Fundamental Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 0	81 A[7:0]	1 A_7	0 A_6	0 A_5	0 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Contrast Control	Double byte command to select one of the contrast steps. Contrast increases as the value increases. (RESET = 7Fh) A[7:0] valid range: 01h to FFh
0	A0/A1	1	0	1	0	0	0	0	X_0	Set Segment Re-map	A0h, X[0]=0b: column address 0 is mapped to SEG0 (RESET) A1h, X[0]=1b: column address 127 is mapped to SEG0
0	A4/A5	1	0	1	0	0	1	0	X_0	Entire Display ON	A4h, X_0=0b: Resume to RAM content display (RESET) Output follows RAM content A5h, X_0=1b: Entire display ON Output ignores RAM content
0	A6/A7	1	0	1	0	0	1	1	X_0	Set Normal/Inverse Display	A6h, X[0]=0b: Normal display (RESET) 0 in RAM: OFF in display panel 1 in RAM: ON in display panel A7h, X[0]=1b: Inverse display 0 in RAM: ON in display panel 1 in RAM: OFF in display panel
0 0	A8 A[7:0]	1 *	0 *	1 A_5	0 A_4	1 A_3	0 A_2	0 A_1	0 A_0	Set Multiplex Ratio	Set MUX ratio to N+1 MUX N=A[5:0] : from 16MUX to 64MUX. RESET = 111111b (i.e. 63d, 64MUX) A[5:0] from 0 to 14 are invalid entry
0 0	AD A[5:4]	1 0	0 0	1 A_5	0 A_4	1 0	1 0	0 0	1 0	Internal I_{REF} Setting	Select external or internal I_{REF}: A[4] = '0': Select external I_{REF} (RESET) A[4] = '1': Enable internal I_{REF} during display ON Internal I_{REF} value setting: A[5] = '0': Internal IREF setting: 19uA, output a maximum I_{SEG}=150uA (RESET) A[5] = '1': Internal I_{REF} setting: 30uA, output a maximum I_{SEG}=240uA
0	AE/AF	1	0	1	0	1	1	1	X_0	Set Display ON/OFF	AEh, X[0]=0b: Display OFF (sleep mode) (RESET) AFh X[0]=1b: Display ON in normal mode
0	B0~B7	1	0	1	1	0	X_2	X_1	X_0	Set Page Start Address for Page Addressing Mode	Set GDDRAM Page Start Address PAGE0~PAGE7 for Page Addressing Mode using X[2:0]. **Note** (1) This command is only for page addressing mode

Fundamental Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	C0/C8	1	1	0	0	X_3	0	0	0	Set COM Output Scan Direction	C0h, X[3]=0b: normal mode (RESET) Scan from COM0 to COM[N –1] C8h, X[3]=1b: remapped mode. Scan from COM[N-1] to COM0 Where N is the Multiplex ratio.
0 0	D3 A[5:0]	1 *	1 *	0 A_5	1 A_4	0 A_3	0 A_2	1 A_1	1 A_0	Set Display Offset	Set vertical shift by COM from 0d~63d. The value is reset to 00h after RESET.
0 0	D5 A[7:0]	1 A_7	1 A_6	0 A_5	1 A_4	0 A_3	1 A_2	0 A_1	1 A_0	Set Display Clock Divide Ratio/Oscillator Frequency	A[3:0] : Define the divide ratio (D) of the display clocks (DCLK): Divide ratio= A[3:0] + 1, RESET is 0000b (divide ratio = 1) A[7:4] : Set the Oscillator Frequency, F_{OSC}. Oscillator Frequency increases with the value of A[7:4] and vice versa. RESET is 1000b. Range: 0000b~1111b. Frequency increases as setting value increases.
0 0	D9 A[7:0]	1 A_7	1 A_6	0 A_5	1 A_4	1 A_3	0 A_2	0 A_1	1 A_0	Set Pre-charge Period	A[3:0] : Phase 1 period of up to 30 DCLK (i.e. 2, 4, 6, …30) Clocks 0 is invalid entry (RESET=2h) A[7:4] : Phase 2 period of up to 30 DCLK (i.e. 2, 4, 6, …30) Clocks 0 is invalid entry (RESET=2h)
0 0	DA A[5:4]	1 0	1 0	0 A_5	1 A_4	1 0	0 0	1 1	0 0	Set COM Pins Hardware Configuration	A[4]=0b, Sequential COM pin configuration A[4]=1b (RESET), Alternative COM pin Configuration A[5]=0b (RESET), Disable COM Left/Right remap A[5]=1b, Enable COM Left/Right remap
0 0	DB A[5:4]	1 0	1 0	0 A_5	1 A_4	1 0	0 0	1 0	1 0	Set V_{COMH} select Level	Set COM select voltage level. A[5:4] | Hex code | V_{COMH} deselect level 00b | 00h | ~ 0.65 x V_{CC} 01b | 10h | ~ 0.71 x V_{CC} 10b | 20h | ~ 0.77 x V_{CC} (RESET) 11b | 30h | ~ 0.83 x V_{CC}
0	E3	1	1	1	0	0	0	1	1	NOP	Command for no operation

Internal Charge Pump Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 0	8D A[7:0]	1 A_7	0 0	0 0	0 1	1 0	1 A_2	0 0	1 A_0	Charge Pump Setting	Enable / Disable internal charge pump: A[2] = 0b, Disable charge pump (RESET) A[2] = 1b, Enable charge pump during display on A[7] | A[0] | Hex code | Charge Pump Mode 0b | 0b | 14h | 7.5V (RESET) 1b | 0b | 94h | 8.5V 1b | 1b | 95h | 9.0V **Note** (1) The Charge Pump must be enabled by the following command sequence: 8Dh ; Charge Pump Setting 14h / 94h / 95h ; Enable Charge Pump AFh; Display ON

Scrolling Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	26/27	0	0	1	0	0	1	1	X_0	Continuous Horizontal Scroll Setup	26h, X[0]=0, Right Horizontal Scroll 27h, X[0]=1, Left Horizontal Scroll (Horizontal scroll by 1 column) A[7:0] : Dummy byte (Set as 00h) B[2:0] : Define start page address 000b – PAGE0 | 011b – PAGE3 | 110b – PAGE6 001b – PAGE1 | 100b – PAGE4 | 111b – PAGE7 010b – PAGE2 | 101b – PAGE5 | C[2:0] : Set time interval between each scroll step in terms of frame frequency 000b – 6 frames | 100b – 3 frames 001b – 32 frames | 101b – 4 frames 010b – 64 frames | 110b – 5 frame 011b – 128 frames | 111b – 2 frame D[2:0] : Define end page address 000b – PAGE0 | 011b – PAGE3 | 110b – PAGE6 001b – PAGE1 | 100b – PAGE4 | 111b – PAGE7 010b – PAGE2 | 101b – PAGE5 | E[6:0] : Define start column address (RESET = 00h) F[6:0] : Define end column address (RESET = 7Fh) **Notes:** (1) The value of D[2:0] must be larger than or equal to B[2:0] (2) The value of F[6:0] must be larger than or equal to E[6:0]
0	A[7:0]	0	0	0	0	0	0	0	0		
0	B[2:0]	0	0	0	0	0	B_2	B_1	B_0		
0	C[2:0]	0	0	0	0	0	C_2	C_1	C_0		
0	D[2:0]	0	0	0	0	0	D_2	D_1	D_0		
0	E[7:0]	0	E_6	E_5	E_4	E_3	E_2	E_1	E_0		
0	F[7:0]	0	F_6	F_5	F_4	F_3	F_2	F_1	F_0		

Scrolling Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	29/2A	0	0	1	0	1	0	X_1	X_0	Continuous Vertical and Horizontal Scroll Setup	29h, X_1X_0=01b : Vertical and Right Horizontal Scroll 2Ah, X_1X_0=10b : Vertical and Left Horizontal Scroll A[0] : Set number of column scroll offset 0b No horizontal scroll 1b Horizontal scroll by 1 column B[2:0] : Define start page address 000b – PAGE0 | 011b – PAGE3 | 110b – PAGE6 001b – PAGE1 | 100b – PAGE4 | 111b – PAGE7 010b – PAGE2 | 101b – PAGE5 C[2:0] : Set time interval between each scroll step in terms of frame frequency 000b – 6 frames | 100b – 3 frames 001b – 32 frames | 101b – 4 frames 010b – 64 frames | 110b – 5 frame 011b – 128 frames | 111b – 2 frame D[2:0] : Define end page address 000b – PAGE0 | 011b – PAGE3 | 110b – PAGE6 001b – PAGE1 | 100b – PAGE4 | 111b – PAGE7 010b – PAGE2 | 101b – PAGE5 E[5:0] : Vertical scrolling offset e.g. E[5:0]= 01h refer to offset =1 row E[5:0] =3Fh refer to offset =63 rows F[6:0] : Define the start column address (RESET = 00h) G[6:0] : Define the end column address (RESET = 7Fh) **Note** (1) The value of D[2:0] must be larger than or equal to B[2:0] (2) The value of E[5:0] must be less than B[6:0] in A3h (3) The value of G[6:0] must be larger than or equal to F[6:0]
0	A[2:0]	0	0	0	0	0	0	0	A_0		
0	B[2:0]	0	0	0	0	0	B_2	B_1	B_0		
0	C[2:0]	0	0	0	0	0	C_2	C_1	C_0		
0	D[2:0]	0	0	0	0	0	D_2	D_1	D_0		
0	E[5:0]	0	0	E_5	E_4	E_3	E_2	E_1	E_0		
0	F[5:0]	0	F_6	F_5	F_4	F_3	F_2	F_1	F_0		
0	G[5:0]	0	G_6	G_5	G_4	G_3	G_2	G_1	G_0		

Scrolling Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	2E	0	0	1	0	1	1	1	0	Deactivate scroll	Stop scrolling that is configured by command 26h/27h/29h/2Ah. **Note** (1) After sending 2Eh command to deactivate the scrolling action, the ram data needs to be rewritten.
0	2F	0	0	1	0	1	1	1	1	Activate scroll	Start scrolling that is configured by the scrolling setup commands :26h/27h/29h/2Ah with the following valid sequences: Valid command sequence 1: 26h ;2Fh. Valid command sequence 2: 27h ;2Fh. Valid command sequence 3: 29h ;2Fh. Valid command sequence 4: 2Ah ;2Fh. For example, if "26h; 2Ah; 2Fh." commands are issued, the setting in the last scrolling setup command, i.e. 2Ah in this case, will be executed. In other words, setting in the last scrolling setup command overwrites the setting in the previous scrolling setup commands.
0	A3	1	0	1	0	0	0	1	1	Set Vertical Scroll Area	A[5:0] : Set No. of rows in top fixed area. The No. of rows in top fixed area is referenced to the top of the GDDRAM (i.e. row 0). [RESET = 0] B[6:0] : Set No. of rows in scroll area. This is the number of rows to be used for vertical scrolling. The scroll area starts in the first row below the top fixed area. [RESET = 64] **Note** (1) A[5:0]+B[6:0] <= MUX ratio (2) B[6:0] <= MUX ratio (3a) Vertical scrolling offset (E[5:0] in 29h/2Ah) < B[6:0] (3b) Set Display Start Line ($X_5X_4X_3X_2X_1X_0$ of 40h~7Fh) < B[6:0] (4) The last row of the scroll area shifts to the first row of the scroll area. (5) For 64d MUX display A[5:0] = 0, B[6:0]=64 : whole area scrolls A[5:0] = 0, B[6:0] < 64 : top area scrolls A[5:0] + B[6:0] < 64 : central area scrolls A[5:0] + B[6:0] = 64 : bottom area scrolls
0	A[5:0]	0	0	A_5	A_4	A_3	A_2	A_1	A_0		
0	B[6:0]	0	B_6	B_5	B_4	B_3	B_2	B_1	B_0		

Scrolling Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	2C/2D	0	0	1	0	1	1	0	X_0	Content Scroll Setup	2Ch, X[0]=0, Right Horizontal Scroll by one column 2Dh, X[0]=1, Left Horizontal Scroll by one column A[7:0] : Dummy byte (Set as 00h) B[2:0] : Define start page address 000b – PAGE0 / 011b – PAGE3 / 110b – PAGE6 001b – PAGE1 / 100b – PAGE4 / 111b – PAGE7 010b – PAGE2 / 101b – PAGE5 C[7:0] : Dummy byte (Set as 01h) D[2:0] : Define end page address 000b – PAGE0 / 011b – PAGE3 / 110b – PAGE6 001b – PAGE1 / 100b – PAGE4 / 111b – PAGE7 010b – PAGE2 / 101b – PAGE5 E[6:0] : Define start column address (RESET = 00h) F[6:0] : Define end column address (RESET = 7Fh) **Note** (1) The value of D[2:0] must be larger than or equal to B[2:0] (2) The value of F[6:0] must be larger than E[6:0] (3) A delay time of 2 frame frequency must be set if sending the command of 2Ch / 2Dh consecutively
0	A[7:0]	0	0	0	0	0	0	0	0		
0	B[2:0]	0	0	0	0	0	B_2	B_1	B_0		
0	C[7:0]	0	0	0	0	0	0	0	1		
0	D[2:0]	0	0	0	0	0	D_2	D_1	D_0		
0	E[7:0]	0	E_6	E_5	E_4	E_3	E_2	E_1	E_0		
0	F[7:0]	0	F_6	F_5	F_4	F_3	F_2	F_1	F_0		

Advance Graphic Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 0	23 A[5:0]	0 *	0 *	1 A_5	0 A_4	0 A_3	0 A_2	1 A_1	1 A_0	Set Fade Out and Blinking	A[5:4] = 00b Disable Fade Out / Blinking Mode[RESET] A[5:4] = 10b Enable Fade Out mode. Once Fade Out mode is enabled, contrast decrease gradually to all pixels OFF. Output follows RAM content when Fade mode is disabled. A[5:4] = 11b Enable Blinking mode. Once Blinking mode is enabled, contrast decrease gradually to all pixels OFF and then contrast increase gradually to normal display. This process loop continuously until the Blinking mode is disabled. A[3:0] : Set time interval for each fade step A[3:0] – Time interval for each fade step 0000b – 8 Frames 0001b – 16 Frames 0010b – 24 Frames : 1111b – 128 Frames Note (1) Refer to section 1.4.1 for details.
0 0	D6 A[0]	1 *	1 *	0 *	1 *	0 *	1 *	1 *	0 A_0	Set Zoom In	A[0] = 0b Disable Zoom in Mode [RESET] A[0] = 1b Enable Zoom in Mode Note (1) The panel must be in alternative COM pin configuration (command DAh A[4] =1) (2) Refer to section 1.4.2 for details.

Note
(1) "*" stands for "Don't care".

9. FUNCTIONAL SPECIFICATION

9.1 Commands

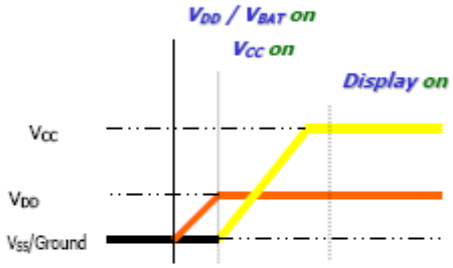
Refer to the Technical Manual for the SSD1306

9.2 Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

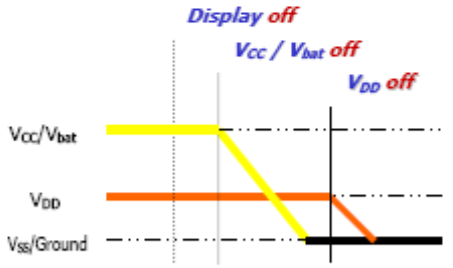
9.2.1 Power up Sequence:

1. Power up V_{DD}
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up V_{CC}/ V_{BAT}
6. Delay 100ms
   (When V_{CC} is stable)
7. Send Display on command



9.2.2 Power down Sequence:

1. Send Display off command
2. Power down V_{CC} / V_{BAT}
3. Delay 100ms
   (When V_{CC} / V_{BAT} is reach 0 and panel is completely discharges)
4. Power down V_{DD}



Note 13:

1) Since an ESD protection circuit is connected between V_{DD} and V_{CC} inside the driver IC, V_{CC} becomes lower than V_{DD} whenever V_{DD} is ON and V_{CC} is OFF.
2) V_{CC} / V_{BAT} should be kept float (disable) when it is OFF.
3) Power Pins (V_{DD}, V_{CC}, V_{BAT}) can never be pulled to ground under any circumstance.
4) V_{DD} should not be power down before V_{CC} / V_{BAT} power down.

9.3 Reset Circuit

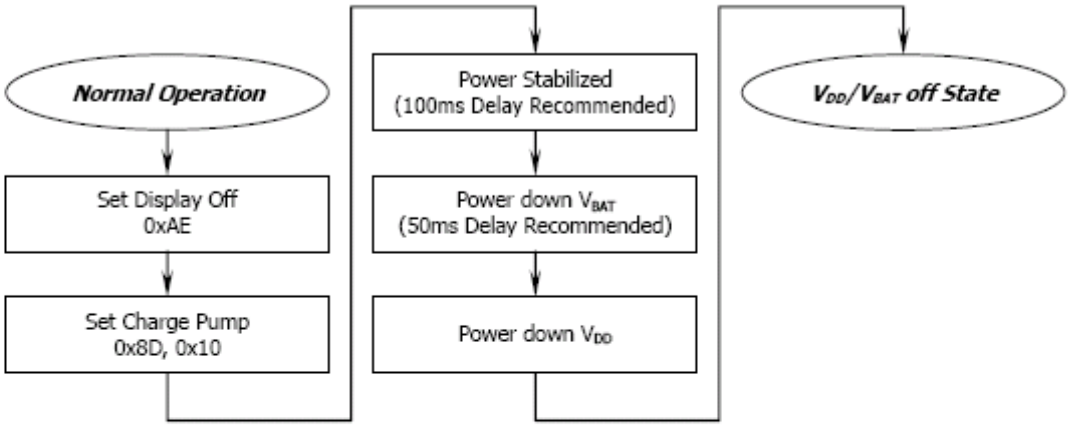
When RES# input is low, the chip is initialized with the following status:

1. Display is OFF
2. 128×64 Display Mode
3. Normal segment and display data column and row address mapping (SEG0 mapped to colum address 00h and COM0 mapped to row address 00h)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 7Fh
9. Normal display mode (Equivalent to A4h command)

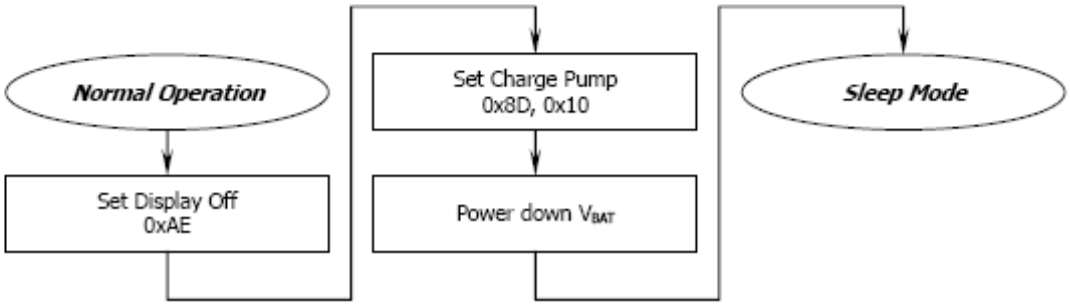
9.4 Actual Application Example

If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

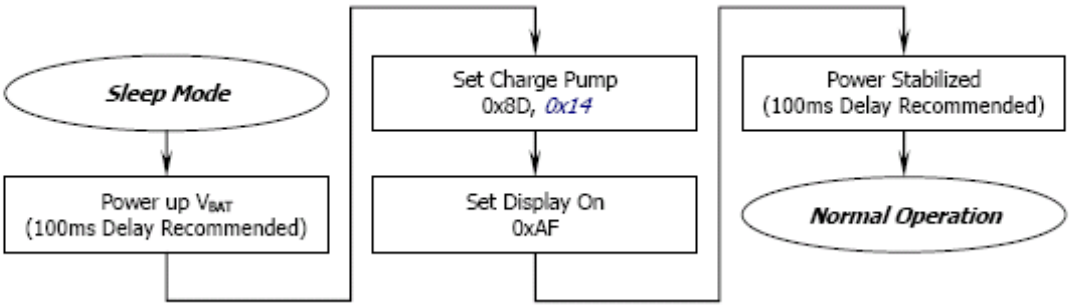
<Power down Sequence>



<Entering Sleep Mode>



<Exiting Sleep Mode>



10. MODULE ACCEPT QUALITY LEVEL (AQL)

10.1 AQL Standard Value: Critical Defect =0.1, Major Defect=0.65; Minor Defect =2.5.

10.2 Inspection Standard: MIL-STD-105E Table Normal Inspection Single Sampling Level II

11. RELIABILITY TEST.

11.1 Contents of Reliability Tests

Item	Conditions	Criteria
High Temperature Operation	70°C, 240 hrs	The operational functions work.
Low Temperature Operation	-40°C, 240 hrs	
High Temperature Storage	85°C, 240 hrs	
Low Temperature Storage	-40°C, 240 hrs	
High Temperature/Humidity Operation	60°C, 90% RH, 120 hrs	
Thermal Shock	-40°C ⇔ 85°C, 24 cycles 60 mins dwell	

* The samples used for the above tests do not include polarizer.
* No moisture condensation is observed during tests.

11.2 Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23±5°C; 55±15% RH.

12. QUALITY DESCRIPTION & APPLICTION NOTE

Please refer to "General Inspection Criteria" document.