8 Bit enhanced USB MCU ch552, ch551

manual

Version: 1D

http://wch.cn

1 Overview

Ch552 chip is an enhanced e8051 core single chip microcomputer compatible with MCS51 instruction set. 79% of its instructions are single byte single cycle instructions, and the average instruction speed is 8-15 times faster than the standard MCS51.

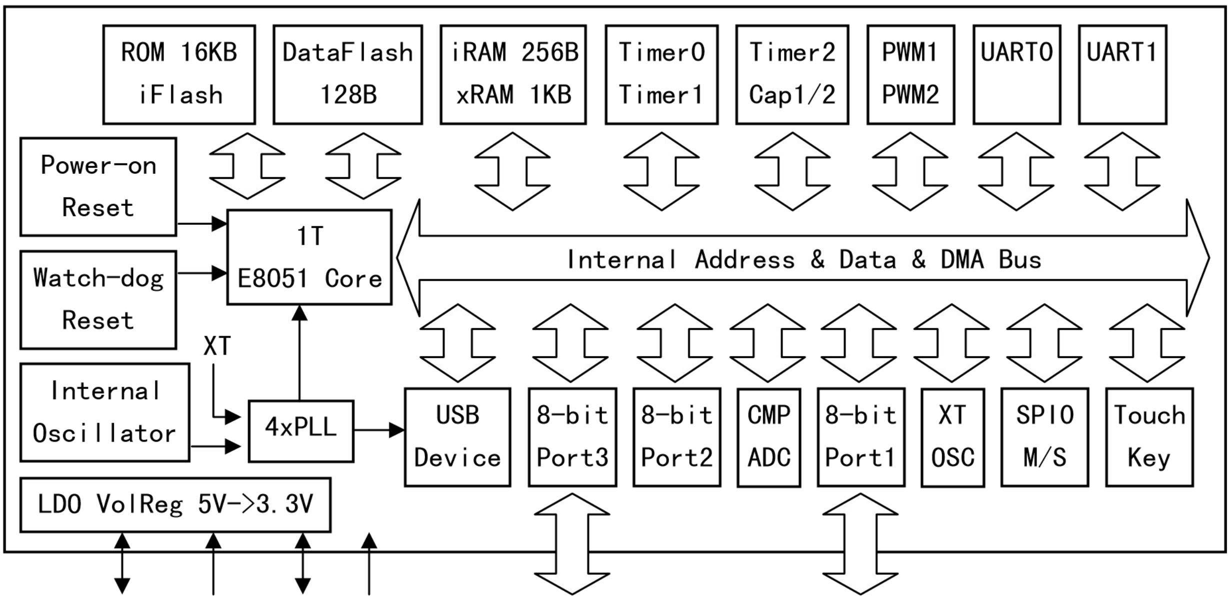
Ch552 supports up to 24MHz system main frequency. It has built-in 16K program memory ROM, 256 byte internal IRAM and 1K byte on-chip xram. Xram supports DMA direct memory access.

The ch552 has built-in ADC analog-to-digital conversion, touch button capacitance detection, three sets of timers and signal capture, PWM, dual asynchronous serial port SPI, USB device controller and full speed transceiver.

Ch551 is a simplified version of ch552. The ROM of program memory is 10K, the on-chip xram is 512 bytes, the asynchronous serial port is only UART0, the package is only SOP16, and the touch button is only 4 channels. Besides, the ADC analog-to-digital conversion module and USB type-C module are removed

Ch552 is the same, you can refer to ch552 manual and materials directly.

model	Program ROM	RAM	DataFlash	USB device	type-C	timer	PWM	Serial port	SPI	ADC	Touch the button
CH552	16KB	1280	128	Full / low speed	Configurable	3group	2group	2group	Master / slave	4road	6passage way
CH551	10KB	768			nothing			1group		nothing	4passage way



Pins: GND VCC V33 RST P30~P37 P10~P17

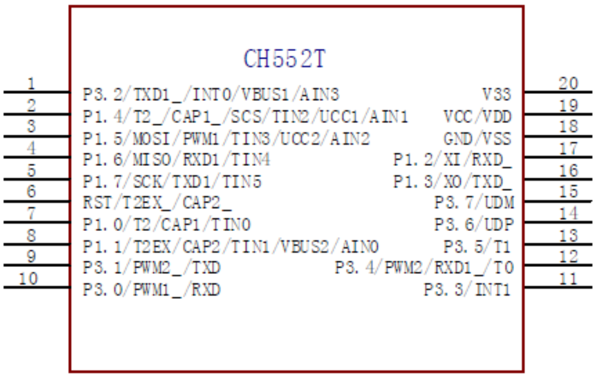
2 Characteristics

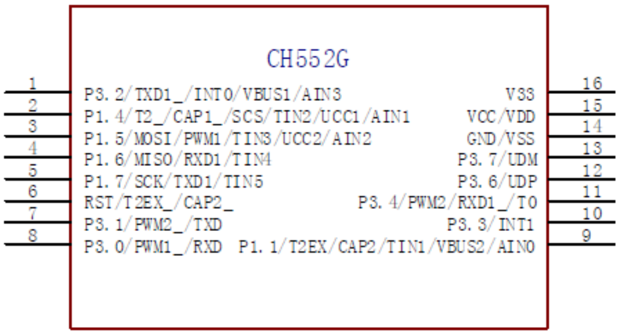
- Core: enhanced e8051 core, compatible with MCS51 instruction set. 79% of its instructions are single byte single cycle instructions. The average instruction speed is

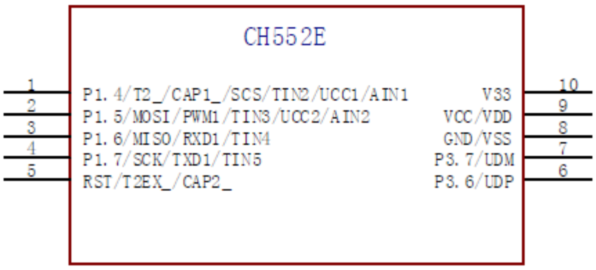
8-15 times faster than the standard MCS51. It has a special xram data replication instruction and double dptr pointer.

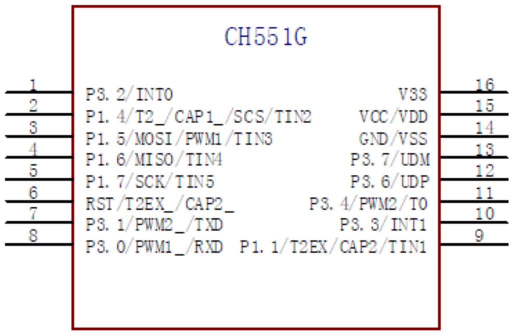
- ROM: 16 KB capacity of multi programmable non-volatile memory ROM, can be used for all program storage space; or can be divided into 14 KB program storage area and 2 kb boot code bootloader / ISP program area.
- DataFlash: 128 byte multi erasable non-volatile data memory, which supports rewriting data in bytes.
- Ram: 256 byte internal RAM, which can be used for fast data storage and stack; 1KB on chip xram can be used for large amount of data temporary storage and DMA direct memory access.
- USB: embedded USB controller and USB transceiver, supporting USB device mode, supporting USB type-C master-slave detection, supporting USB 2.0 full speed 12mbps or low speed 1.5mbps.FIFO is built-in and supports 64 bytes of data packets.
- Timer: three groups of timers, t0 / T1 / T2 is the standard MCS51 timer.
- Capture: timer T2 is extended to support 2-way signal capture.
- PWM: 2 sets of PWM output, pwm1 / pwm2 is 2-way 8-bit PWM output.
- UART: two groups of asynchronous serial ports, both support higher communication baud rate, UART0 is the standard MCS51 serial port.
- SPI: SPI controller has built-in FIFO, clock frequency up to half of the system's main frequency Fsys, supports serial data input and output simplex multiplexing, and supports master / slave mode.
- ADC: 4-channel 8-bit A / D converter, supporting voltage comparison.
- Touch key: 6-channel capacitance detection, support up to 15 touch buttons, support independent timing interrupt.
- GPIO: supports up to 17 GPIO pins (including Xi / XO, RST and USB signal pins).
- Interrupt: supports 14 groups of interrupt signal sources, including 6 groups of interrupts (INT0, T0, INT1, T1, etc.) compatible with standard MCS51 UART0, T2), and extended 8 groups of interrupts (spi0, tkey, USB, ADC, uart1, pwmx, GPIO, wdog), in which GPIO interrupt can be selected from 7 pins.
- Watch dog: 8 bits can preset watchdog timer wdog, support timing interrupt.
- Reset: support 4 kinds of reset signal source, built-in power on reset, support software reset and watchdog overflow reset, optional pin external input reset.
- Clock: built in 24 MHz clock source, which can support external crystal by multiplexing GPIO pins.
- Power: built in 5V to 3.3V low voltage differential voltage regulator, supporting 5V or 3.3V or even 2.8V power supply voltage.It supports low-power sleep, USB, UART0, uart1, spi0 and part of GPIO external wake-up.
- The chip has a unique ID number.

3 Packaging









Packaging form	Width of plastic body		Pin spacing		Package description	Order model
TSSOP-20	4.40 mm	173mil	0.65 mm	25mil	Thin small 20 foot patch	CH552T
SOP-16	3.9mm	150mil	1.27 mm	50mil	Standard 16 pin patch	CH552G
MSOP-10	3.0mm	118mil	0.50 mm	19.7mil	Mini 10 pin patch	CH552E
SOP-16	3.9mm	150mil	1.27 mm	50mil	Standard 16 pin patch	CH551G

4, pin

Pin number			Pin name	Other function names (left function is preferred)	Description of other functions
TSSOP 20	SOP16	MSOP10			
19	15	9	VCC	VDD	The power input terminal needs to be connected with 0.1uF power decoupling capacitor.
20	16	10	V33		Internal USB power regulator output and internal USB power input. When the power supply voltage is less than 3.6V, it is connected with VCC input external power supply. When the power supply voltage is greater than 3.6V, an external 0.1uF power decoupling capacitor is connected
18	14	8	GND	VSS	Common ground terminal.
6	6	5	RST	RST/T2EX_/CAP2_	A pin with an underscores suffix is a mapping of pins with the same name without underscores. Rst pin has built-in pull-down resistor; other GPIO has pull-up resistor by default Rst: external reset input. T2: external count input / clock output of timer / counter 2. T2ex: timer / counter 2 overload / capture input. Cap1, CAP2: capture input 1 and 2 of timer / counter 2. Tin0-tin5: 0 ၉ - 5 ၉ - 5 ၉ channel touch button capacitance detection input. Analog signal input of channel ain0 ～ ain3:0 ၉ - 3 ◌ာ - 3 ◌ာ. UCC1, ucc2: USB type-C bidirectional configuration channel. Vbus1, vbus2: USB type-C bus voltage detection input. 11. XO: external crystal oscillation input end, reverse phase output end. RXD, TXD: UART0 serial data input, serial data output. SCS, MoSi, miso, SCK: spi0 interface, SCS is chip selection input, MoSi is master output / slave input, miso is host input /SCK is a serial clock. Pwm1, pwm2: pwm1 output, pwm2 output. Rxd1, txd1: uart1 serial data input, serial data output INT0, INT1: external interrupt 0, external interrupt 1 input. T0, T1: external input of timer 0 and timer 1. UDM, UDP: D -, D + signal terminal of USB device. Note: P3.6 and P3.7 use V33 as I / O power supply internally, so the high level of input and output can only reach V33 voltage, not 5V
7	-	-	P1.0	T2/CAP1/TIN0	
8	9	-	P1.1	T2EX/CAP2/TIN1/VBUS2/AIN0	
17	-	-	P1.2	XI/RXD_	
16	-	-	P1.3	XO/TXD_	
2	2	1	P1.4	T2_/CAP1_/SCS/TIN2/UCC1/AIN1	
3	3	2	P1.5	MOSI/PWM1/TIN3/UCC2/AIN2	
4	4	3	P1.6	MISO/RXD1/TIN4	
5	5	4	P1.7	SCK/TXD1/TIN5	
10	8	-	P3.0	PWM1_/RXD	
9	7	-	P3.1	PWM2_/TXD	
1	1	-	P3.2	TXD1_/INT0/VBUS1/AIN3	
11	10	-	P3.3	INT1	
12	11	-	P3.4	PWM2/RXD1_/T0	
13	-	-	P3.5	T1	
14	12	6	P3.6	UDP	
15	13	7	P3.7	UDM	

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5 Special function register SFR

The following abbreviations may be used in the description of registers in this manual:

Abbreviations	describe
RO	Represents the access type: read only
WO	Indicates the access type: write only, invalid value read
RW	Represents the type of access: readable and writable
H	End with a hexadecimal number
B	End with a binary number

5.1 introduction and address distribution of SFR

Ch552 uses SFR to control and manage the equipment and set the working mode.

SFR occupies the 80h FFH address range of internal data storage space and can only be accessed by direct address instruction.The register with address of x0h or x8h can be addressed by bit, so as to avoid modifying the value of other bits when accessing a specific bit; other registers with addresses other than 8 times can only be accessed by byte.

Some sfrs can only write data in safe mode, while they are read-only in non secure mode, such as global_CFG、

CLOCK_CFG、WAKE_CTRL。

Some sfrs have one or more aliases, for example: spi0_CK_SE/SPI0_S_PRE。

The partial address corresponds to multiple independent sfrs, such as safe_MOD/CHIP_ID、ROM_CTRL/ROM_STATUS。

Ch552 contains 8051 standard SFR registers and other device control registers.The specific SFR is shown in the table below.

Table 5.1 special function register table

SFR	0、8	1、9	2、A	3、B	4、C	5、D	6、E	7、F
0xF8	SPI0_STAT	SPI0_DATA	SPI0_CTRL	SPI0_CK_SE SPI0_S_PRE	SPI0_SETUP		RESET_KEEP	WDOG_COUNT
0xF0	B							
0xE8	IE_EX	IP_EX	UEP4_1_MOD	UEP2_3_MOD	UEP0_DMA_L	UEP0_DMA_H	UEP1_DMA_L	UEP1_DMA_H
0xE0	ACC	USB_INT_EN	USB_CTRL	USB_DEV_AD	UEP2_DMA_L	UEP2_DMA_H	UEP3_DMA_L	UEP3_DMA_H
0xD8	USB_INT_FG	USB_INT_ST	USB_MIS_ST	USB_RX_LEN	UEP0_CTRL	UEP0_T_LEN	UEP4_CTRL	UEP4_T_LEN
0xD0	PSW	UDEV_CTRL	UEP1_CTRL	UEP1_T_LEN	UEP2_CTRL	UEP2_T_LEN	UEP3_CTRL	UEP3_T_LEN
0xC8	T2CON	T2MOD	RCAP2L	RCAP2L	TL2	TH2	T2CAP1L	T2CAP1H
0xC	SCON1	SBUF1	SBAUD1	TKEY_CTRL	TKEY_DATL	TKEY_DATH	PIN_FUNC	GPIO_IE

0								
0xB8	IP	CLOCK_CFG						
0xB0	P3	GLOBAL_CFG						
0xA8	IE	WAKE_CTRL						
0xA0	P2	SAFE_MOD CHIP_ID	XBUS_AUX					
0x98	SCON	SBUF	ADC_CFG	PWM_DATA2	PWM_DATA1	PWM_CTRL	PWM_CK_SE	ADC_DATA
0x90	P1	USB_C_CTRL	P1_MOD_OC	P1_DIR_PU			P3_MOD_OC	P3_DIR_PU
0x88	TCON	TMOD	TL0	TL1	TH0	TH1	ROM_DATA_L	ROM_DATA_H
0x80	ADC_CTRL	SP	DPL	DPH	ROM_ADDR_L	ROM_ADDR_H	ROM_CTRL ROM_STATUS	PCON

Note: (1) the red text indicates that the address can be bit by bit; (2) the following is the corresponding description of the color box

(grey)	Address register
(purple)	Spi0 related register
(light blue)	ADC related register
(orange)	Touch key related registers
(green)	USB related registers
(blue)	Timer / counter 2 related register
(peach)	Port setting related registers
(cyan)	Pwm1 and pwm2 related registers
(yellow)	Uart1 related register
(teal)	Flash-ROM related registers

5.2 classification and reset value of SFR

Table 5.2 SFR description and reset values

Functional classification	name	address	describe	reset value
System setting related registers	B	F0h	B register	0000 0000b
	ACC	E0h	accumulator	0000 0000b
	PSW	D0h	Program status register	0000 0000b
	GLOBAL_CFG	B1h	Global configuration register (in ch552 bootloader state)	1010 0000b
			Global configuration register (in ch552 application state)	1000 0000b
			Global configuration register (in	1110

			ch551 bootloader state)	0000b
			Global configuration register (in ch551 application state)	1100 0000b
	CHIP_ID	A1h	Ch552 chip ID code (read only)	0101 0010b
			Ch551 chip ID code (read only)	0101 0001b
	SAFE_MOD	A1h	Safe mode control register (write only)	0000 0000b
	DPH	83h	Data address pointer 8 bits high	0000 0000b
	DPL	82H	Data address pointer lower 8 bits	0000 0000b
	DPTR	82H	DPL and DPH constitute 16 bit SFR	0000h
	SP	81h	Stack pointer	0000 0111b
Clock, sleep and power control registers	WDOG_COUNT	FFh	Watchdog count register	0000 0000b
	RESET_KEEP	FEh	Reset holding register (under power on reset state)	0000 0000b
	CLOCK_CFG	B9h	System clock configuration register	1000 0011b
	WAKE_CTRL	A9h	Sleep wake control register	0000 0000b
	PCON	87h	Power control register (under power on reset state)	0001 0000b
Interrupt control related register	IP_EX	E9h	Extended interrupt priority control register	0000 0000b
	IE_EX	E8h	Extended interrupt enable register	0000 0000b
	GPIO_IE	C7h	GPIO interrupt enable register	0000 0000b
	IP	B8h	Interrupt priority control register	0000 0000b
	IE	A8h	Interrupt enable register	0000 0000b
Flash-ROM related registers	ROM_DATA_H	8Fh	Flash-ROM data register high byte	xxxx xxxxb
	ROM_DATA_L	8Eh	Flash-ROM data register low byte	xxxx xxxxb
	ROM_DATA	8Eh	ROM_DATA_L and ROM_DATA_H constitutes a 16 bit SFR	xxxxh
	ROM_STATUS	86h	Flash-ROM status register (read only)	0000 0000b
	ROM_CTRL	86h	Flash-ROM control register (write only)	0000 0000b
	ROM_ADDR	85h	Flash-ROM address register high	xxxx

	_H		byte	xxxxb
	ROM_ADDR_L	84h	Flash-ROM address register low byte	xxxx xxxxb
	ROM_ADDR	84h	ROM_ADDR_L and ROM_ADDR_H constitutes a 16 bit SFR	xxxxh
Port setting related registers	PIN_FUNC	C6h	Pin function selection register	1000 0000b
	XBUS_AUX	A2h	External bus auxiliary setting register	0000 0000b
	P3_DIR_PU	97h	P3 port direction control and pull up enable register	1111 1111b
	P3_MOD_OC	96h	P3 port output mode register	1111 1111b
	P1_DIR_PU	93h	P1 port direction control and pull up enable register	1111 1111b
	P1_MOD_OC	92h	P1 port output mode register	1111 1111b
	P3	B0h	P3 port I / O register	1111 1111b
	P2	A0h	P2 port output register	1111 1111b
	P1	90h	P1 port I / O register	1111 1111b

Timer / counter 0And 1 Correlation register	TH1	8Dh	Timer1 count high byte	xxxx xxxxb
	TH0	8Ch	Timer0 counts high bytes	xxxx xxxxb
	TL1	8Bh	Timer1 counts low bytes	xxxx xxxxb
	TL0	8Ah	Timer0 counts low bytes	xxxx xxxxb
	TMOD	89h	Timer0 / 1 mode register	0000 0000b
	TCON	88H	Timer0 / 1 control register	0000 0000b
UART0 Correlation register	SBUF	99H	UART0 data register	xxxx xxxxb
	SCON	98H	UART0 control register	0000 0000b
Timer / counter 2Correlation register	T2CAP1H	CFh	Timer2 captures 1 data high byte (read only)	xxxx xxxxb
	T2CAP1L	CEh	Timer2 capture 1 data low byte (read only)	xxxx xxxxb
	T2CAP1	CEh	T2cap1l and t2cap1h constitute a 16 bit SFR	xxxxh
	TH2	CDh	Timer2 counter high byte	0000

				0000b
	TL2	CCh	Timer2 counter low byte	0000 0000b
	T2COUNT	CCh	TL2 and Th2 constitute a 16 bit SFR	0000h
	RCAP2H	CBh	Count overload / capture 2 data register high byte	0000 0000b
	RCAP2L	CAh	Count overload / capture 2 data register low byte	0000 0000b
	RCAP2	CAh	Rcap2l and rcap2h constitute a 16 bit SFR	0000h
	T2MOD	C9h	Timer2 mode register	0000 0000b
	T2CON	C8h	Timer2 control register	0000 0000b
Pwm1 and pwm2 related registers	PWM_CK_SE	9Eh	PWM clock frequency division setting register	0000 0000b
	PWM_CTRL	9Dh	PWM Control Register	0000 0010b
	PWM_DATA 1	9Ch	Pwm1 data register	xxxx xxxxb
	PWM_DATA 2	9Bh	Pwm2 data register	xxxx xxxxb
SPI0 Correlation register	SPI0_SETUP	FCh	Spi0 setting register	0000 0000b
	SPI0_S_PRE	FBh	Spi0 slave mode preset data register	0010 0000b
	SPI0_CK_SE	FBh	Spi0 clock frequency division setting register	0010 0000b
	SPI0_CTRL	FAh	Spi0 control register	0000 0010b
	SPI0_DATA	F9h	Spi0 data transceiver register	xxxx xxxxb
	SPI0_STAT	F8h	Spi0 status register	0000 1000b
UART1 Correlation register	SBAUD1	C2h	Uart1 baud rate setting register	xxxx xxxxb
	SBUF1	C1h	Uart1 data register	xxxx xxxxb
	SCON1	C0h	Uart1 control register	0100 0000b
ADC Correlation register	ADC_DATA	9Fh	ADC data register	xxxx xxxxb
	ADC_CFG	9Ah	ADC configuration register	0000 0000b
	ADC_CTRL	80h	ADC control register	x000 0000b
Touch key	TKEY_DATH	C5h	Touch key data high byte (read only)	0000

related registers				0000b
	TKEY_DATL	C4h	Touch key data low byte (read only)	xxxx xxxxb
	TKEY_DAT	C4h	TKEY_Datl and tkey_Dath forms a 16 bit SFR	00xxh
	TKEY_CTRL	C3h	Touch key control register	x000 0000b
USB Correlation register	UEP1_DMA_H	EFh	Endpoint 1 buffer start address high byte	0000 00xxb
	UEP1_DMA_L	EEh	Endpoint 1 buffer start address low byte	xxxx xxxxb
	UEP1_DMA	EEh	UEP1_DMA_L and uep1_DMA_H constitutes a 16 bit SFR	0xxxh
	UEP0_DMA_H	EDh	Endpoint 0 and 4 buffer start address high byte	0000 00xxb
	UEP0_DMA_L	ECh	Endpoint 0 and 4 buffer start address low byte	xxxx xxxxb
	UEP0_DMA	ECh	UEP0_DMA_L and uep0_DMA_H constitutes a 16 bit SFR	0xxxh
	UEP2_3_MOD	EBh	Endpoint 2,3 mode control register	0000 0000b
	UEP4_1_MOD	EAh	Endpoint 1,4 mode control register	0000 0000b
	UEP3_DMA_H	E7h	Endpoint 3 buffer start address high byte	0000 00xxb
	UEP3_DMA_L	E6h	Endpoint 3 buffer start address low byte	xxxx xxxxb
	UEP3_DMA	E6h	UEP3_DMA_L and uep3_DMA_H constitutes a 16 bit SFR	0xxxh
	UEP2_DMA_H	E5h	Endpoint 2 buffer start address high byte	0000 00xxb
	UEP2_DMA_L	E4h	Endpoint 2 buffer start address low byte	xxxx xxxxb
	UEP2_DMA	E4h	UEP2_DMA_L and uep2_DMA_H constitutes a 16 bit SFR	0xxxh
	USB_DEV_AD	E3h	USB device address register	0000 0000b
	USB_CTRL	E2h	USB control register	0000 0110b
	USB_INT_EN	E1h	USB interrupt enable register	0000 0000b
	UEP4_T_LEN	DFh	Endpoint 4 transmit length register	0xxx xxxxb
	UEP4_CTRL	DEh	Endpoint 4 control register	0000 0000b
	UEP0_T_LEN	DDh	Endpoint 0 send length register	0xxx xxxxb

	UEP0_CTRL	DCh	Endpoint 0 control register	0000 0000b
	USB_RX_LEN	DBh	USB receive length register (read only)	0xxx xxxxb
	USB_MIS_ST	DAh	USB miscellaneous status register (read only)	xx10 1000b
	USB_INT_ST	D9h	USB interrupt status register (read only)	00xx xxxxb
	USB_INT_FG	D8h	USB interrupt flag register	0010 0000b
	UEP3_T_LEN	D7h	Endpoint 3 transmit length register	0xxx xxxxb
	UEP3_CTRL	D6h	Endpoint 3 control register	0000 0000b
	UEP2_T_LEN	D5h	End point send register length 2	0000 0000b
	UEP2_CTRL	D4h	Endpoint 2 control register	0000 0000b
	UEP1_T_LEN	D3h	Endpoint 1 transmit length register	0xxx xxxxb
	UEP1_CTRL	D2h	Endpoint 1 control register	0000 0000b
	UDEV_CTRL	D1h	USB device port control register	10xx 0000b
	USB_C_CTRL	91h	USB type-C configuration channel control register	0000 0000b

5.3 General 8051 register

Table 5.3.1 list of general 8051 registers

name	address	describe	reset value
B	F0h	B register	00h
A、ACC	E0h	accumulator	00h
PSW	D0h	Program status register	00h
GLOBAL_CFG	B1h	Global configuration register (in ch552 bootloader state)	A0h
		Global configuration register (in ch552 application state)	80h
		Global configuration register (in ch551 bootloader state)	E0h
		Global configuration register (in ch551 application state)	C0h
CHIP_ID	A1h	Ch552 chip ID code (read only)	52h
		Ch551 chip ID code (read only)	51h
SAFE_MOD	A1h	Safe mode control register (write only)	00h
PCON	87h	Power control register (under power on reset	10h

		state)	
DPH	83h	Data address pointer 8 bits high	00h
DPL	82H	Data address pointer lower 8 bits	00h
DPTR	82H	DPL and DPH constitute 16 bit SFR	0000h
SP	81h	Stack pointer	07h

B register:

position	name	visit	describe	reset value
[7:0]	B	RW	Arithmetic operation register, mainly used for multiplication and division, can be addressed by bit	00h

A accumulator
(a, ACC)

position	name	visit	describe	reset value
[7:0]	A/ACC	RW	Arithmetic accumulator, bit addressable	00h

Program status register (PSW)

position	name	visit	describe	reset value
7	CY	RW	Carry flag bit: used to record the carry or borrow bit of the highest bit when performing arithmetic operation and logic operation instruction; when performing 8-bit addition operation, carry the highest bit, then the position bit, otherwise clear to zero; when performing 8-bit subtraction operation, if borrow, the position bit, otherwise clear zero; logic instruction can make the position bit or clear zero	0
6	AC	RW	Auxiliary carry flag bit: record the carry or borrow bit from the low 4 bits to the high 4 bits during the operation of the addition and subtraction method, and AC is set, otherwise it is cleared	0
5	F0	RW	General flag bit 0 that can be addressed by bit: the user can define it by himself, and can be reset or set by software	0
4	RS1	RW	Register group select bit high	0
3	RS0	RW	Register group select bit low	0
2	OV	RW	Overflow flag bit: when the operation result exceeds 8 bits in addition and subtraction, OV is set to 1, flag overflow, otherwise clear 0	0
1	F1	RW	Bit addressable general flag bit 1: user can define it by himself, and can be reset or set by software	0
0	P	RO	Parity flag bit: record the parity of 1 in accumulator a after the instruction is executed. If an odd 1 is set, P is set, and even 1 is p cleared	0

The state of the processor is stored in the state register PSW, which supports bitwise addressing.The carry flag bit is included in the status word, which is used for BCD code processing auxiliary carry flag bit, parity flag bit, overflow flag bit, as well as rs0 and RS1 for working register group selection.

The region of the working register group can be accessed directly or indirectly.

Table 5.3.2 selection table of RS1 and rs0 working registers

RS1	RS0	Working register group
0	0	0Group (00h-07h)
0	1	1Group (08h-0fh)
1	0	2Group (10h-17h)
1	1	3Group (18h-1fh)

Table 5.3.3 operation affecting flag bit (x indicates that flag bit is related to operation result)

operation	CY	OV	AC	operation	CY	OV	AC
ADD	X	X	X	SETB C	1		
ADDC	X	X	X	CLR C	0		
SUBB	X	X	X	CPL C	X		
MUL	0	X		MOV C, bit	X		
DIV	0	X		ANL C, bit	X		
DA A	X			ANL C,/bit	X		
RRC A	X			ORL C, bit	X		
RLC A	X			ORL C,/bit	X		
CJNE	X						

Data address pointer (dptr)

position	name	visit	describe	reset value
[7:0]	DPL	RW	Data pointer low byte	00h
[7:0]	DPH	RW	Data pointer high byte	00h

DPL and DPH constitute a 16 bit data pointer dptr, which is used to access the xram data memory or program memory. The actual dptr corresponds to two groups of physical 16 bit data pointers dptr0 and dptr1, which are composed of Xbus_DPS dynamic selection in aux.

Stack pointer:

position	name	visit	describe	reset value
[7:0]	SP	RW	Stack pointer, mainly used for program calls and interrupt calls, as well as data in and out of the stack	07h

Stack specific functions: protect breakpoints and protect the scene, according to the principle of first in and then out.When entering the stack, the SP pointer will automatically add 1 to save the data or breakpoint information; when leaving the stack, the SP pointer will point to the data unit, and the SP pointer will automatically decrease by 1.The initial value of SP after reset is 07h, and the corresponding default stack storage starts from 08h.

5.4 Special register

Global configuration register (Global_CFG), which can only be written in safe mode:

position	name	visit	describe	reset value
[7:6]	retain	RO	For ch552, it is a fixed value of 10	10B
[7:6]	retain	RO	For ch551, it is a fixed value of 11	11B
5	bBOOT_LOAD	RO	Boot loader status bit, used to distinguish ISP boot program status or application program status: set to 1 when power on, and clear 0 when software is reset. For the chip with ISP bootloader, if this bit is 1, it means that the software has never been reset, which is usually the ISP boot program status running after power on; if this bit is 0, it indicates that the software has been reset, which is usually the application program status	1
4	bSW_RESET	RW	Software reset control bit: Set 1 to cause software reset and hardware to reset automatically	0
3	bCODE_WE	RW	Write allowed bits of flash-ROM and DataFlash: if this bit is 0, it is write protected; if it is 1, flash-ROM and data can be rewritten	0
2	bDATA_WE	RW	Write allowed bits in the DataFlash area of flash-ROM: if the bit is 0, it is write protected; if it is 1, the DataFlash area can be rewritten	0
1	bLDO3V3_OFF	RW	Disable control bit of LDO in USB power conditioner: if this bit is 0, LDO is allowed, and 3.3V voltage can be generated by 5V power supply USB and internal clock oscillator; if it is 1, LDO is disabled, V33 pin must input external 3.3V power supply	0
0	bWDOG_EN	RW	Watchdog reset enable bit: if this bit is 0, watchdog is only used as timer; if this bit is 1, watchdog reset will be generated when timer overflow	0

Chip ID code (chip_ID)：

position	name	visit	describe	reset value
[7:0]	CHIP_ID	RO	For ch552, it is a fixed value of 52h, which is used to identify the chip	52h
[7:0]	CHIP_ID	RO	For a fixed chip, the value is ch51h	51h

Safe mode control register (safe_MOD)：

position	name	visit	describe	reset value
[7:0]	SAFE_MOD	WO	Used to enter or terminate security mode	00h

Some sfrs can only write data in safe mode, while they are always read-only in non secure mode.Steps to enter safe mode:

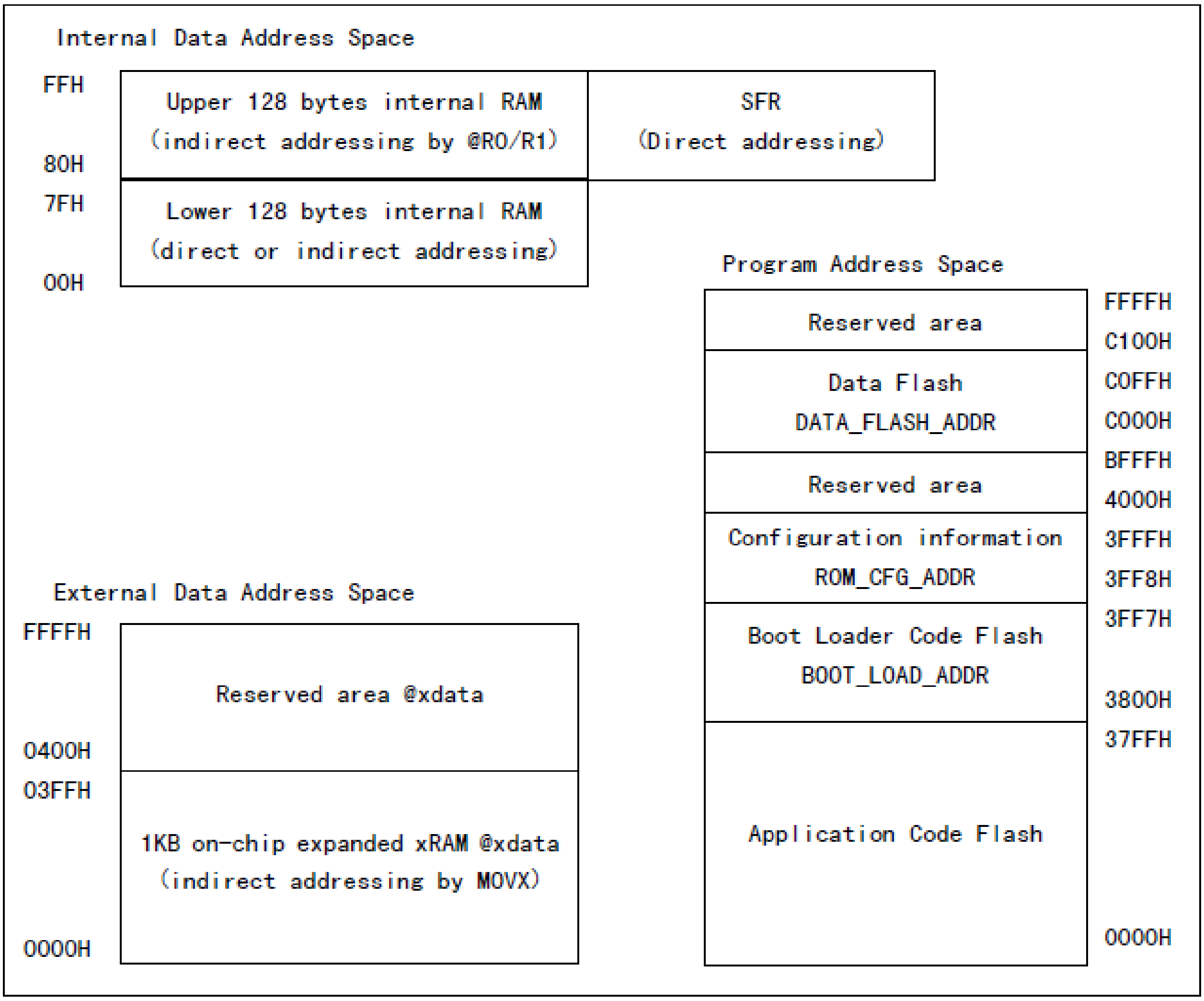
(1) Write 55h to the register;
(2) And then write AAH to the register;
(3) After that, about 13 to 23 main frequency cycles of the system are in safe mode, and one or more security classes can be rewritten within the validity period
SFR or ordinary SFR;
(4) The safety mode will be automatically terminated after the expiration date;
(5) , or write any value to the register to terminate safe mode ahead of time.

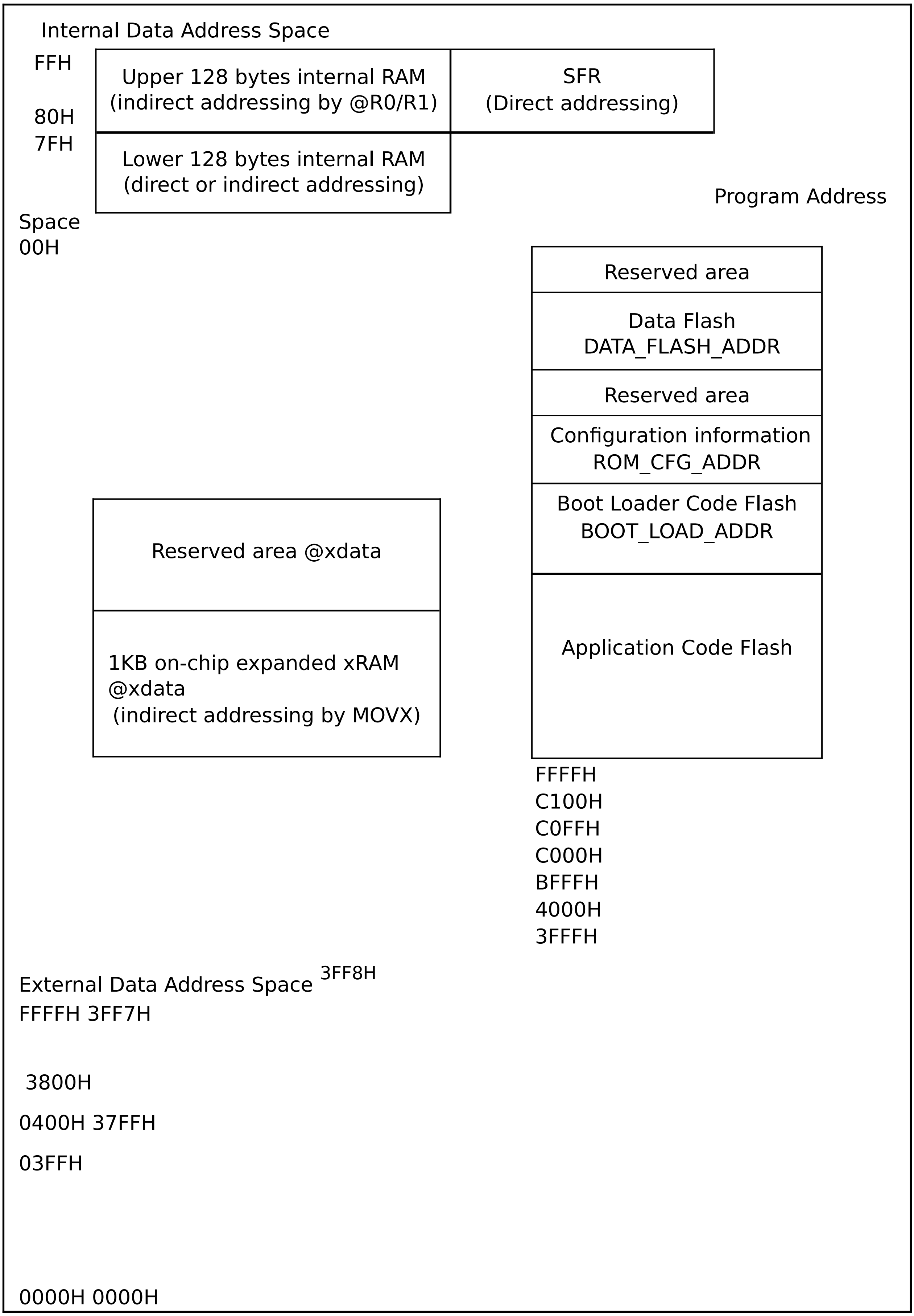
6 Memory structure

6.1 Memory space

The addressing space of ch552 is divided into program storage space, internal data storage space and external data storage space.

Figure 6.1 memory structure





Internal Data Address Space
FFH
Upper 128 bytes internal RAM
(indirect addressing by @R0/R1)
SFR
(Direct addressing)
80H
7FH
Lower 128 bytes internal RAM
(direct or indirect addressing)
Space
00H
Program Address
Reserved area
Data Flash
DATA_FLASH_ADDR
Reserved area
Configuration information
ROM_CFG_ADDR
Boot Loader Code Flash
BOOT_LOAD_ADDR
Application Code Flash
Reserved area @xdata
1KB on-chip expanded xRAM
@xdata
(indirect addressing by MOVX)
FFFFH
C100H
C0FFH
C000H
BFFFH
4000H
3FFFH
External Data Address Space
3FF8H
FFFFH 3FF7H
3800H
0400H 37FFH
03FFH
0000H 0000H

6.2 Program storage space

The program storage space is 64KB, as shown in Figure 6.1, of which 16kb is used for ROM, including code flash area for saving instruction code and configuration information area for configuration information.

Code flash includes application code of low address area and bootstrap code of high address area, which can also be combined to save single application code.

For ch551, the application code area of code flash is only 10KB.

ROM is iflashGammaProcess: for the finished product after the blank ROM is formally packaged, it can be programmed for about 200 times under 5V power supply.

The data flash address range is c000h to c0ffh (only the even address is valid, actually there is a storage unit every other byte). It only supports single byte (8-bit) read and write operations, and the data remains unchanged after the chip is powered down.Data flash supports about 10000 erasures. It is recommended to use it evenly. It is forbidden to write more than 10k times to the same storage unit. If there are more erasures, it is recommended to use ch558 or ch546 / 7.

Configuration information includes four groups of 16 bit data from 3ff8h to 3ffffh, and the last three groups are read-only units, providing chip ID.The configuration data at 3ff8h address is set by the programmer as required, refer to table 6.2.

Table 6.2 description of flash-ROM configuration information

Bit address	Bit name	explain	recommended value
15	Code_Protect	Code and data protection mode in flash-ROM: 0-It is forbidden to read by the programmer, and the program is confidential; 1-read-out is allowed	0/1
14	No_Boot_Load	Enable bootloader boot code boot mode: 0-Start from the application program of 0000H address; 1-Boot from 3800h address	1
13	En_Long_Reset	Additional delay reset during enable power on reset: 0-Standard short reset, 1-wide reset, additional 44ms reset time	0
12	En_RST_RESET	Enable RST pin as manual reset input pin: 0-disable; 1-enable RST	0
[11:10]	retain	(automatically set to 00 by the programmer as required)	00
9	Must_1	(automatically set to 1 by programmer as required)	1
8	Must_0	(automatically set to 0 by the programmer as required)	0
[7:0]	All_1	(automatically set to FFH by programmer as required)	FFh

6.3 The internal data storage space is 256 bytes, as shown in Figure 6.1. It has been used for SFR and IRAM, and IRAM is used for stack

It can be subdivided into working register r0-r7, bit variable bdata, byte variable data, IDATA, etc.The external data storage space is 64KB, as shown in Figure 6.1. Part of the external data storage space is used for 1KB on-chip expansion of xram, and the rest is reserved area.

For ch551, the on-chip expanded xram is only 512 bytes.

6.4 flash-ROM register

Table 6.4 list of flash-ROM operation registers

name	address	describe	reset value
ROM_DATA_H	8Fh	Flash-ROM data register high byte	Xxh
ROM_DATA_L	8Eh	Flash-ROM data register low byte	Xxh
ROM_DATA	8Eh	ROM_DATA_L and ROM_DATA_H constitutes a 16 bit SFR	xxxxh
ROM_STATUS	86h	Flash-ROM status register (read only)	00h
ROM_CTRL	86h	Flash-ROM control register (write only)	00h
ROM_ADDR_H	85h	Flash-ROM address register high byte	Xxh
ROM_ADDR_L	84h	Flash-ROM address register low byte	Xxh
ROM_ADDR	84h	ROM_ADDR_L and ROM_ADDR_H constitutes a 16 bit SFR	xxxxh

Flash-ROM address register (ROM_ADDR)：

position	name	visit	describe	reset value
[7:0]	ROM_ADDR_H	RW	Flash-ROM address high byte	Xxh
[7:0]	ROM_ADDR_L	RW	Flash-ROM address is low byte and only supports even address. For data flash, the actual offset address 00h-7fh must be shifted left 1 bit to even address 00h / 02h / 04HAfter ~ FEH, they were implanted	Xxh

Flash-ROM data register (ROM_DATA)：

position	name	visit	describe	reset value
[7:0]	ROM_DATA_H	RW	High byte of data to be written in flash-ROM	Xxh
[7:0]	ROM_DATA_L	RW	Flash-ROM data to be written low byte, for DataFlash, is to write data bytes or read data bytes	Xxh

Flash-ROM control register (ROM_CTRL)：

position	name	visit	describe	reset value
[7:0]	ROM_CTRL	WO	Flash-ROM control register	00h

Flash-ROM status register (ROM_STATUS)：

position	name	visit	describe	reset value
7	retain	RO	retain	0
6	bROM_ADDR_	RO	Flash-ROM write address valid status bits:	0

	OK		If the bit is 0, the parameter is invalid; if it is 1, the address is valid	
[5:2]	retain	RO	retain	0000b
1	bROM_CMD_ERR	RO	Flash-ROM operation command error status bit: If the bit is 0, the command is valid; if it is 1, it is unknown	0
0	retain	RO	retain	0

6.5 flash-ROM operation steps

1. Write the flash-ROM code area and write double byte data to the target address

(1) If flash-ROM code needs to be written, 5V power supply voltage must be selected;

(2) , enable safe mode, safe_MOD = 55h； SAFE_MOD = 0AAh；

(3) Set the global configuration register global_CFG enable write enable (BCODE)_We or bdata_We corresponds to code or data);

(4) Setting address register ROM_Addr, write 16 bit target address (the lowest bit is always 0);

(5) Set the data register ROM_Data, write 16 bits of data to be written, and the sequence of steps (4) and (5) can be adjusted;

(6) Set the operation control register ROM_When the CTRL is 09ah, the write operation is executed, and the program automatically stops running during the operation;

(7) After the operation is completed, the program will resume running and query the status register ROM_Status can view the operation status; if you want to write multiple data, cycle steps (4), (5), (6), (7);

(8) Safe mode again_MOD = 55h； SAFE_MOD = 0AAh；

(9) Set the global configuration register global_CFG on write protect (BCODE_WE=0，bDATA_WE=0)。

2. Write the data flash data area and write single byte data to the target address

(1) , enable safe mode, safe_MOD = 55h； SAFE_MOD = 0AAh；

(2) Set the global configuration register global_CFG enable write enable (bdata_We corresponds to data);

(3) Setting address register ROM_Addr, write 16 bit target address, the actual offset address 00h-7fh must be shifted left 1 bit to even address 00h / 02h / 04HThe final address was c000h / c002h / C004;

(4) Set the data register ROM_DATA_50. Write 8 bits of data to be written, and the sequence of steps (3) and (4) can be adjusted;

(5) Set the operation control register ROM_When the CTRL is 09ah, the write operation is executed, and the program automatically stops running during the operation;

(6) After the operation is completed, the program will resume running and query the status register ROM_Status can view the operation status; if you want to write multiple data, cycle steps (3), (4), (5), (6);

(7) , enter safe mode again, safe_MOD = 55h； SAFE_MOD = 0AAh；

(8) Set the global configuration register global_CFG on write protect (BCODE_WE=0，bDATA_WE=0)。

3. Read the data flash data area and read single byte data from the target address:

(1) Setting address register ROM_Addr, write 16 bit target address, the actual offset address 00h-7fh must be shifted left 1 bit to even address, the final address is c000h / c002h / C004;
(2) Set the operation control register ROM_When the CTRL is 08eh, read operation will be executed, and the program will be suspended automatically during the operation;
(3) After the operation is completed, the program will resume running and query the status register ROM_Brom in status_CMD_Err can view the operation status; if the command is valid, the 8-bit data read will be saved in the data register ROM_DATA_In L;
(4) If you want to read more than one data, cycle through steps (1), (2), (3).

4. Read flash-ROM:
Read the code or data of the target address directly by using MOVC instruction or by pointer to program storage space.

6.6 On board programming and ISP download

When the configuration information code_When protect = 1, the code in flash-ROM of ch552 chip and data in data flash can be read and written by external programmer through synchronous serial interface_When protect = 0, code and data in flash-ROM The data in flash is protected and cannot be read out, but it can be erased. After erasing, the code protection will be removed when power is turned on again.

When the bootloader bootloader is preset in ch552 chip, ch552 can support USB or asynchronous serial port and other ISP download methods to load applications; but without bootloader, ch552 can only be written into bootloader or application program by external special programmer.In order to support on-board programming, 5V power supply voltage must be used temporarily, and 4 connecting pins between ch552 and programmer should be reserved in the circuit, and the minimum necessary connection pins are P1.4, P1.6 and P1.7.

Table 6.6.1 connection pins to Programmer

Pin	GPIO	Pin description
RST	RST	Reset the control pin in the programming state, and the high level is allowed to enter the programming state
SCS	P1.4	Chip selection input pin in programming state (necessary), default high level, low level is valid
SCK	P1.7	Clock input pin in programming state (necessary)
MISO	P1.6	Data output pin in programming state (necessary)

Note: whether programming on board or downloading program through serial port or USB, 5V power supply voltage must be used temporarily.

6.7 Chip unique ID number

Each single chip microcomputer has a unique ID number when it leaves the factory, that is, the chip identification number.The ID data is 5 bytes in total, and is stored in 3ffah to 3fffh addresses in the configuration information area.Among them, 3ffbh address is reserved unit, 16 bit data of 3ffch and 3ffeh address and 8-bit data of 3ffah address are merged into 40 bit chip ID data.

Table 6.7.1 chip ID address table

Program space address	ID data description

3FFAh、3FF Bh	The last word data of ID is the highest byte and reserved byte of 40 bit ID number
3FFCh、3FF Dh	The first word data of ID is the lowest byte and the second lower byte of ID number
3FFEh、3FFF h	ID secondary word data, followed by the ID number of the next high byte, high byte

The ID data can be obtained by reading code flash.ID number can be used with download tool to encrypt the target program. In general application, only the first 32 bits of ID number can be used, that is, 8-bit data of 3ffah address can be ignored.

7 Power management, sleep and reset

7.1 External power input

Ch552 chip is built-in 5V to 3.3V low voltage differential voltage regulator, supporting external 5V or 3.3V or even 2.8V power supply voltage input. Refer to the table below for two power supply voltage input modes.

External supply voltage	VCC pin voltage: external voltage 3V ~ 5V	V33 pin voltage: internal voltage 3.3V
3.3V or 3V includes less than 3.6V	The external 3.3V voltage input to the voltage regulator must be grounded with a decoupling capacitor of not less than 0.1uF	Input external 3.3V as the internal power supply, must be connected to the ground not less than 0.1uF decoupling capacitance
5V Including more than 3.6V	Input external 5V voltage to the voltage regulator, must be grounded to no less than 0.1uF decoupling capacitor	The 3.3V output of the internal voltage regulator and the 3.3V internal working power input must be grounded with a decoupling capacitor of no less than 0.1uF

After power on or system reset, ch552 is running by default.On the premise that the performance meets the requirements, the power consumption can be reduced by properly reducing the main frequency of the system.When ch552 does not need to run at all, the PD in PCON can be set to enter sleep state. In sleep state, external wake-up can be performed through USB, UART0, uart1, spi0 and some GPIO.

7.2 Power and sleep control register

Table 7.2.1 list of power and sleep control registers

name	address	describe	reset value
WDOG_COUNT	FFh	Watchdog count register	00h
RESET_KEEP	FEh	Reset holding register	00h
WAKE_CTRL	A9h	Sleep wake control register	00h
PCON	87h	Power control register	10h

Watchdog count register (wdog_COUNT)：

position	name	visit	describe	reset value
[7:0]	WDOG_COUNT	RW	Watch dog current count, overflow when 0ffh turns to 00h, when overflow, it will automatically set the interrupt flag bwdog_IF_To is 1	00h

Reset hold register (reset_KEEP)：

position	name	visit	describe	reset value
[7:0]	RESET_KEEP	RW	Reset the holding register, the value can be artificially modified, except that power on reset can clear it, any other reset does not affect the value	00h

Sleep wake control register (wake_CTRL), which can only be written in safe mode:

position	name	visit	describe	reset value
7	bWAK_BY_USB	RW	USB event wake enable, this bit is 0 to disable wake-up	0
6	bWAK_RXD1_LO	RW	Uart1 receive input low level wake-up enable, this bit is 0 to prohibit wake-up.According to bauart1_PIN_X = 0 / 1 select rxd1 or rxd1_Pin	0
5	bWAK_P1_5_LO	RW	P1.5 low level wake-up enable, 0 disable wake-up	0
4	bWAK_P1_4_LO	RW	P1.4 low level wake-up enable, 0 disable wake-up	0
3	bWAK_P1_3_LO	RW	P1.3 low level wake-up enable, 0 disable wake-up	0
2	bWAK_RST_HI	RW	Rst high level wake-up enable, 0 disable wake-up	0
1	bWAK_P3_2E_3L	RW	P3.2 edge change and p3.3 low-level wake-up enable, 0 disable wake-up	0
0	bWAK_RXD0_LO	RW	UART0 receive input low-level wake-up enable, 0 disable wake-up.According to bauart0_PIN_X = 0 / 1 select rxd0 or rxd0_Pin	0

Power control register (PCON)

position	name	visit	describe	reset value
7	SMOD	RW	When timer 1 is used to generate UART0 baud rate, select UART0 mode 1 2Baud rate of 3: 0-slow mode; 1-fast mode	0
6	retain	RO	retain	0
5	bRST_FLAG1	R0	Chip last reset flag high	0
4	bRST_FLAG0	R0	Chip last reset flag low	1
3	GF1	RW	General flag bit 1: the user can define it by himself, and can be reset or set by software	0

2	GF0	RW	General flag bit 0: the user can define it by himself, and can be reset or set by software	0
1	PD	RW	Sleep mode enable, set 1 to sleep, wake up hardware automatically reset	0
0	retain	RO	retain	0

Table 7.2.2 description of chip latest reset flag

bRST_FLAG1	bRST_FLAG0	Reset flag description
0	0	Software reset, source: BSW_Reset = 1 and (bboot)_Load = 0 or bwlog_EN=1)
0	1	Power on reset, source: VCC pin voltage is lower than detection level
1	0	Watchdog reset, source: bwdog_EN = 1 and watchdog timeout overflow
1	1	Manual reset of external pin, source: en_RST_Reset = 1 and RST input high level

7.3 Reset control

There are three reset sources: ch552 and external reset after reset.

7.3.1 Power on reset

Power on reset por is generated by on-chip voltage detection circuit.POR circuit continuously monitors the power supply voltage of VCC pin. When the power supply voltage is lower than the detection level vpot, the power on reset is generated, and the hardware automatically delays tpor to maintain the reset state. After the delay is over, ch552 runs.

Only power on reset causes ch552 to reload configuration information and reset_Keep, other thermal reset does not affect.

7.3.2 External reset

The external reset is generated by a high level added to the rst pin.When the configuration information en_RST_When reset is 1 and the duration of high level on RST pin is greater than trst, the reset process is triggered.When the external high-level signal is cancelled, the hardware automatically delays trdl to maintain the reset state. After the delay ends, ch552 starts to execute from address 0.

7.3.3 Software reset

Ch552 supports internal software reset so that CPU status can be reset and run again without external intervention.Set global configuration register Global_BSW in CFG_If the reset value is 1, the software can be reset, and trdl will be automatically delayed to maintain the reset state. After the delay is over, ch552 will be executed from address 0, and BSW_The reset bit is automatically cleared by hardware.

When BSW_When reset is set to 1, if bboot_Load = 0 or bwlog_If en = 1, then brst after reset_Flag1 / 0 will indicate software reset; when BSW_When reset is set to 1, if bboot_Load = 1 and bwlog_EN = 0, then brst_Instead of a reset flag, Flag10 will remain unchanged.

For the chip with ISP boot program, after power on reset, run the boot program first. The program resets the chip according to the need to switch to the application program state. This software reset only causes bboot_Load clearing does not affect brst_Status of flag1 / 0 (due to bboot before reset_Load = 1), so when switching to application state, brst_Flag1 / 0 is still in power on reset state.

7.3.4 Watchdog reset

Watchdog reset is generated when watchdog timer time-out overflows.The watchdog timer is an 8-bit counter whose clock frequency is the system main frequency Fsys / 65536. When 0ffh turns to 00h, overflow signal will be generated.

Watchdog timer overflow signal will trigger the interrupt flag bwlog_IF_When to is 1, the interrupt flag is reloading wdog_It is automatically cleared when count or entering the corresponding interrupt service program.

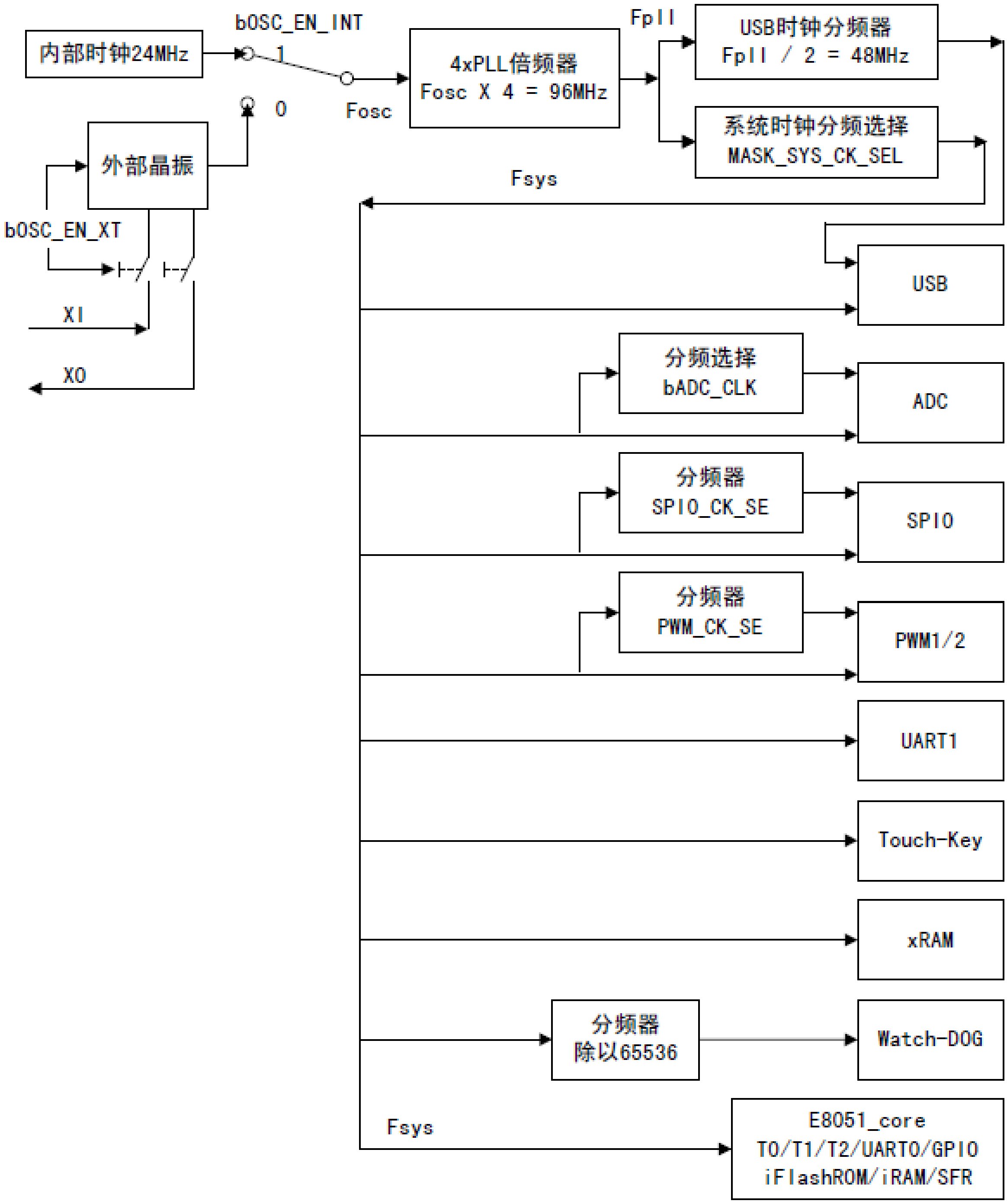
Through the_Count writes different initial count values to achieve different timing periods.At 6mhz frequency, the watchdog timing period twdc is about 2.8s at 00h and 1.4s at 80h.It is halved at 12 MHz.

If watchdog timer overflows, bwlog_When en = 1, watchdog reset is generated, and trdl is automatically delayed to maintain the reset state. After the delay, ch552 starts to execute from address 0.

When bwlog_When en = 1, wdog must be reset in time to avoid being reset by watchdog_Count to avoid overflow.

8, system clock

8.1 Clock block diagram 8.1.1 clock system and structure diagram



The internal clock or external clock is selected as the original clock FOSC, and then it is generated by 4xpll frequency doubling. Finally, the system clock Fsys and the clock fusb4x of USB module are obtained by two groups of frequency dividers.The system clock Fsys is directly provided to each module of ch552.

8.2 Register description table 8.2.1 clock control register list

name	address	describe	reset value
CLOCK_CFG	B9h	System clock configuration register	83h

System clock configuration register (clock_CFG), which can only be written in safe mode:

position	name	visit	describe	reset value
7	bOSC_EN_INT	RW	Internal clock oscillator enable, this bit is 1 to enable internal clock oscillator and select internal clock; this bit is 0 to turn off internal clock oscillator and select external crystal oscillator to provide clock	1
6	bOSC_EN_XT	RW	If this bit is 1, then P1.2 / p1.3 pin is used as Xi / XO and the oscillator is enabled, quartz crystal or ceramic oscillator should be connected between Xi and XO; if this bit is 0, the external oscillator will be closed	0
5	bWDOG_IF_TO	RO	Watchdog timer interrupt flag bit, this bit is 1 to indicate interrupt, triggered by timer overflow signal; 0 indicates no interrupt.This bit reloads the watchdog count register wdog_Automatically reset when count or after entering the corresponding interrupt service program	0
4	bROM_CLK_FAST	RW	Flash-ROM reference clock frequency selection: 0 - normal (if FOSC > = 16mhz); 1-acceleration (if FOSC < 16mhz)	0
3	bRST	R0	Rst pin status input bit	0
[2:0]	MASK_SYS_CK_SEL	RW	Refer to table 8.2.2 below for system clock frequency selection	011b

Table 8.2.2 system main frequency selection table

MASK_SYS_CK_SEL	System main frequency Fsys	The relation between FXT and crystal frequency	Fsys when FOSC = 24MHz
000	Fpll / 512	Fxt / 128	187.5KHz
001	Fpll / 128	Fxt / 32	750KHz
010	Fpll / 32	Fxt / 8	3MHz
011	Fpll / 16	Fxt / 4	6MHz
100	Fpll / 8	Fxt / 2	12MHz
101	Fpll / 6	Fxt / 1.5	16MHz
110	Fpll / 4	Fxt / 1	24MHz
111	Fpll / 3	Fxt / 0.75	Keep, disable

8.3 Clock configuration

The internal clock is used by default after ch552 chip is powered on, and the internal clock frequency is 24MHz.You can use the clock_CFG selects internal clock or external crystal oscillator clock. If external crystal oscillator is turned off, Xi and XO pins can be used as P1.2 and p1.3 common I / O ports.If an external crystal oscillator is used to provide the clock, the crystals should be bridged between Xi and XO pins, and oscillation capacitors should be connected to GND for Xi and XO pins respectively; if the clock signal is input directly from the outside, the input should be from Xi pin, and XO pin should be suspended.

Original clock frequency FOSC = BOSC_EN_INT ? 24MHz : Fxt
PLL frequency FPLL = FOSC * 4 = 96mhz USB
clock frequency fusb4x = FPLL / 2 = 48mhz
Refer to table 8.2.2 for the main frequency of the system. After reset, FOSC = 24MHz, FPLL = 96mhz, fusb4x = 48mhz, Fsys = 6mhz.

The steps of switching to the external crystal oscillator to provide clock are as follows:

(1) Enter the safe mode, step 1 safe_Mod = 55h; step 2: safe_MOD = AAh;
(2) Use bit or operation to lock_BOSC in CFG_EN_When XT is set to 1, other bits remain unchanged and crystal oscillator is enabled;
(3) Delay several milliseconds, usually 5ms-10ms, waiting for the crystal oscillator to work stably;
(4) Enter the safe mode again, step 1 safe_Mod = 55h; step 2: safe_MOD = AAh;
(5) Use bit and operation to lock_BOSC in CFG_EN_Int clear 0, other bits remain unchanged, switch to external clock;
(6) Turn off the security mode and turn off the safe mode_Mod writes any value to terminate safe mode ahead of time.

The steps to modify the main frequency of the system are as follows:

(1) Enter the safe mode, step 1 safe_Mod = 55h; step 2: safe_MOD = AAh;
(2) , to clock_The new value is written in CFG;
(3) Turn off the security mode and turn off the safe mode_Mod writes any value to terminate safe mode ahead of time.

remarks:

(1) If the USB module is used, the fusb4x must be 48mhz, and when using full speed USB, the main frequency of the system Fsys is not less than
6mhz; when using low-speed USB, the main frequency of the system is not less than 1.5MHz.
(2) The lower system clock frequency Fsys is preferred to reduce the dynamic power consumption of the system and widen the working temperature range.
(3) The internal clock oscillator is powered by V33 power supply, so the change of V33 voltage, especially the low voltage, will affect the internal clock frequency.

9, interruption

Ch552 chip supports 14 groups of interrupt signal sources, including 6 groups of interrupts compatible with standard MCS51: INT0, T0, INT1, T1, UART0, T2, and 8 extended interrupts: spi0, tkey, USB, ADC, uart1, pwmx, GPIO, wdog. GPIO interrupt can be selected from 7 I / O pins.

9.1 Register description

Table 9.1.1 interrupt vector table

Interrupt source	Entrance address	interrupt number	describe	Default priority order
INT_NO_INT0	0x0003	0	External interrupt 0	high priority

INT_NO_TMR 0	0x000B	1	Timer 0 interrupt	A kind of A kind of A kind of A kind of A kind of A kind of A kind of A kind of A kind of A kind of A kind of Low priority
INT_NO_INT1	0x0013	2	External interrupt 1	
INT_NO_TMR 1	0x001B	3	Timer 1 interrupt	
INT_NO_UART 0	0x0023	4	UART0 interrupt	
INT_NO_TMR 2	0x002B	5	Timer 2 interrupt	
INT_NO_SPI0	0x0033	6	Spi0 interrupt	
INT_NO_TKEY	0x003B	7	Touch the timer interrupt button	
INT_NO_USB	0x0043	8	USB interrupt	
INT_NO_ADC	0x004B	9	ADC interrupt	
INT_NO_UART 1	0x0053	10	Uart1 interrupt	
INT_NO_PWM X	0x005B	11	Pwm1 / pwm2 interrupt	
INT_NO_GPIO	0x0063	12	GPIO interrupt	
INT_NO_WDO G	0x006B	13	Watchdog timer interrupt	

Table 9.1.2 list of interrupt related registers

name	address	describe	reset value
IP_EX	E9h	Extended interrupt priority control register	00h
IE_EX	E8h	Extended interrupt enable register	00h
GPIO_IE	C7h	GPIO interrupt enable register	00h
IP	B8h	Interrupt priority control register	00h
IE	A8h	Interrupt enable register	00h

Interrupt enable register (ie)

position	name	visit	describe	reset value
7	EA	RW	Global interrupt enable control bit, which is 1 and E_If DIS is 0, interrupts are allowed; if this bit is 0, all interrupt requests are masked	0
6	E_DIS	RW	Global interrupt disable control bit, which is 1 to block all interrupt requests; if this bit is 0 and EA is 1, interrupt is allowed.This bit is usually used to temporarily disable interrupts during flash-ROM operations	0
5	ET2	RW	Timer 2 interrupt enable bit, this bit is 1, allow T2 interrupt; 0 mask	0
4	ES	RW	Asynchronous serial port 0 interrupt enable bit, this bit is 1, allow UART0 interrupt; 0 mask	0
3	ET1	RW	Timer 1 interrupt enable bit, this bit is 1 to allow T1	0

			interrupt; 0 mask	
2	EX1	RW	External interrupt 1 enable bit, which is 1 allows INT1 interrupt; is 0 masked	0
1	ET0	RW	Timer 0 interrupt enable bit, this bit is 1, allow t0 interrupt; 0 mask	0
0	EX0	RW	External interrupt 0 enable bit, this bit is 1 to allow INT0 interrupt; it is 0 masked	0

Extended interrupt enable register (ie_EX)：

position	name	visit	describe	reset value
7	IE_WDOG	RW	Watchdog timer interrupt enable bit, this bit is 1 to allow wdog interrupt; it is 0 shielded	0
6	IE_GPIO	RW	GPIO interrupt enable bit, which is 1 to allow GPIO_Enabled interrupt in IE; blocks GPIO for 0_All interrupts in IE	0
5	IE_PWMX	RW	Pwm1 / pwm2 interrupt enable bit, which is 1 to allow pwm1 / 2 interrupt and 0 mask	0
4	IE_UART1	RW	Asynchronous serial port 1 interrupt enable bit, this bit is 1, allow uart1 interrupt; 0 mask	0
3	IE_ADC	RW	ADC ADC interrupt enable bit, which is 1 to allow ADC interrupt; 0 mask	0
2	IE_USB	RW	USB interrupt enable bit, which is 1 to allow USB interrupt and 0 to shield	0
1	IE_TKEY	RW	Touch the button timer interrupt enable bit, which is 1 to allow timing interrupt and 0 to mask	0
0	IE_SPI0	RW	Spi0 interrupt enable bit, this bit is 1 to allow spi0 interrupt; it is 0 mask	0

GPIO interrupt enable register (GPIO_IE)：

position	name	visit	describe	reset value
7	bIE_IO_EDGE	RW	GPIO edge interrupt mode enable: This bit is 0 to select the level interrupt mode. If the GPIO pin inputs the active level, then boi is selected_INT_Act is 1 and interrupt is requested all the time, GPIO input is invalid, and the level of Bi is Io_INT_Act is 0 and interrupt request is cancelled; This bit is 1 to select the edge interrupt mode. When the GPIO pin inputs a valid edge, the interrupt flag bio is generated_INT_The interrupt flag can not be reset by software, and can only be reset or level interrupt mode or enter the corresponding interrupt service program	0
6	bIE_RXD1_LO	RW	This bit is 1 enable uart1 receive pin interrupt (level mode low level is valid, edge mode	0

			falling edge is valid); this bit is 0 disable.According to bauart1_PIN_X = 0 / 1 select rxd1 or rxd1_Pin	
5	bIE_P1_5_LO	RW	This bit is 1 enable P1.5 interrupt (level mode low level is valid, edge mode falling edge is valid); this bit is 0 disable	0
4	bIE_P1_4_LO	RW	This bit is 1 enable P1.4 interrupt (level mode low level is valid, edge mode falling edge is effective); this bit is 0 disable	0
3	bIE_P1_3_LO	RW	This bit is 1 enable p1.3 interrupt (level mode low level is valid, edge mode falling edge is effective); this bit is 0 disable	0
2	bIE_RST_HI	RW	This bit is 1 enable RST interrupt (level mode high level is valid, edge mode rising edge is valid); this bit is 0 disable	0
1	bIE_P3_1_LO	RW	This bit is 1 enable P3.1 interrupt (level mode low level is valid, edge mode falling edge is effective); this bit is 0 disable	0
0	bIE_RXD0_LO	RW	This bit is 1 to enable UART0 receive pin interrupt (level mode low level is valid, edge mode falling edge is valid); this bit is 0 disable.According to bauart0_PIN_X = 0 / 1 select rxd0 or rxd0_Pin	0

Interrupt priority control register (IP)

position	name	visit	describe	reset value
7	PH_FLAG	RO	High priority interrupt execution flag bit	0
6	PL_FLAG	RO	Low priority interrupt execution flag bit	0
5	PT2	RW	Timer 2 interrupt priority control bit	0
4	PS	RW	UART0 interrupt priority control bit	0
3	PT1	RW	Timer 1 interrupt priority control bit	0
2	PX1	RW	Interrupt priority control bit of external interrupt 1	0
1	PT0	RW	Timer 0 interrupt priority control bit	0
0	PX0	RW	Interrupt priority control bit of external interrupt 0	0

Extended interrupt priority control register (IP_EX)：

position	name	visit	describe	reset value
7	bIP_LEVEL	RO	The current interrupt nesting level flag bit. If this bit is 0, it means no interrupt or nesting 2Level 1 interrupt; if this bit is 1, it indicates the current nested level 1 interrupt	0
6	bIP_GPIO	RW	GPIO interrupt priority control bit	0
5	bIP_PWMX	RW	Pwm1 / pwm2 interrupt priority control bit	0

4	bIP_UART1	RW	Uart1 interrupt priority control bit	0
3	bIP_ADC	RW	ADC interrupt priority control bit	0
2	bIP_USB	RW	USB interrupt priority control bit	0
1	bIP_TKEY	RW	Touch the key timer interrupt priority control bit	0
0	bIP_SPI0	RW	Spi0 interrupt priority control bit	0

IP and IP_Ex register is used to set interrupt priority. If a bit is set to 1, the corresponding interrupt source is set as high priority; if a bit is cleared to 0, the corresponding interrupt source is set as low priority.For the same level interrupt source, the system has the default priority order, which is shown in table 9.1.1.Where pH_Flag and PL_Flag combination indicates the priority of the current interrupt.

Table 9.1.3 current interrupt priority status indication

PH_FLAG	PL_FLAG	Current interrupt priority status
0	0	Currently non disruptive
0	1	Currently executing low priority interrupt
1	0	High priority interrupt is currently executing
1	1	Unexpected state, unknown error

10, I / O ports

10.1 introduction to GPIO

Ch552 provides up to 17 I / O pins, some of which have multiplexing function.The input and output of ports P1 and P3 can be addressed bit by bit.Port P2 is an internal port, which is only used to select the xram page for MOVX access with R0 or R1.

If the pin is not configured for multiplexing, the default is the general I / O pin status.When used as a general-purpose digital I / O, all I / O ports have real "read modify write" function, and support setb or CLR operation instructions to independently change the direction of some pins or port level.

10.2 GPIO register

All registers and bits in this section are represented in a common format: the lowercase "n" represents the serial number of the port (n = 1 or 3), while the lowercase "X" represents the serial number of the bit (x = 0, 1, 2, 3, 4, 5, 6, 7).

Table 10.2.1 list of GPIO registers

name	address	describe	reset value
P1	90h	P1 port I / O register	FFh
P1_MOD_OC	92h	P1 port output mode register	FFh
P1_DIR_PU	93h	P1 port direction control and pull up enable register	FFh
P2	A0h	P2 port output register	FFh
P3	B0h	P3 port I / O register	FFh
P3_MOD_OC	96h	P3 port output mode register	FFh
P3_DIR_PU	97h	P3 port direction control and pull up enable register	FFh
PIN_FUNC	C6h	Pin function selection register	80h

XBUS_AUX	A2h	Bus auxiliary setting register	00h

PN port I / O register (PN)

position	name	visit	describe	reset value
[7:0]	Pn.0～Pn.7	RW	PN. X pin status input and data output bits can be addressed by bit	FFh

PN port output mode register (PN_MOD_OC)：

position	name	visit	describe	reset value
[7:0]	Pn_MOD_OC	RW	PN. X pin output mode setting: 0-push-pull output; 1-open drain output	FFh

PN port direction control and pull up enable register (PN_DIR_PU)：

position	name	visit	describe	reset value
[7:0]	Pn_DIR_PU	RW	In push-pull output mode, PN. X pin direction control: 0-Input; 1-output; in open drain output mode, the pull-up resistance of PN. X pin enables control: 0-It is forbidden to pull up the resistor; 1 - enable the pull-up resistor	FFh

By PN_MOD_OC [x] and PN_DIR_Pu [x] combination realizes the relevant configuration of PN port, as follows.

Table 10.2.2 port configuration register combination

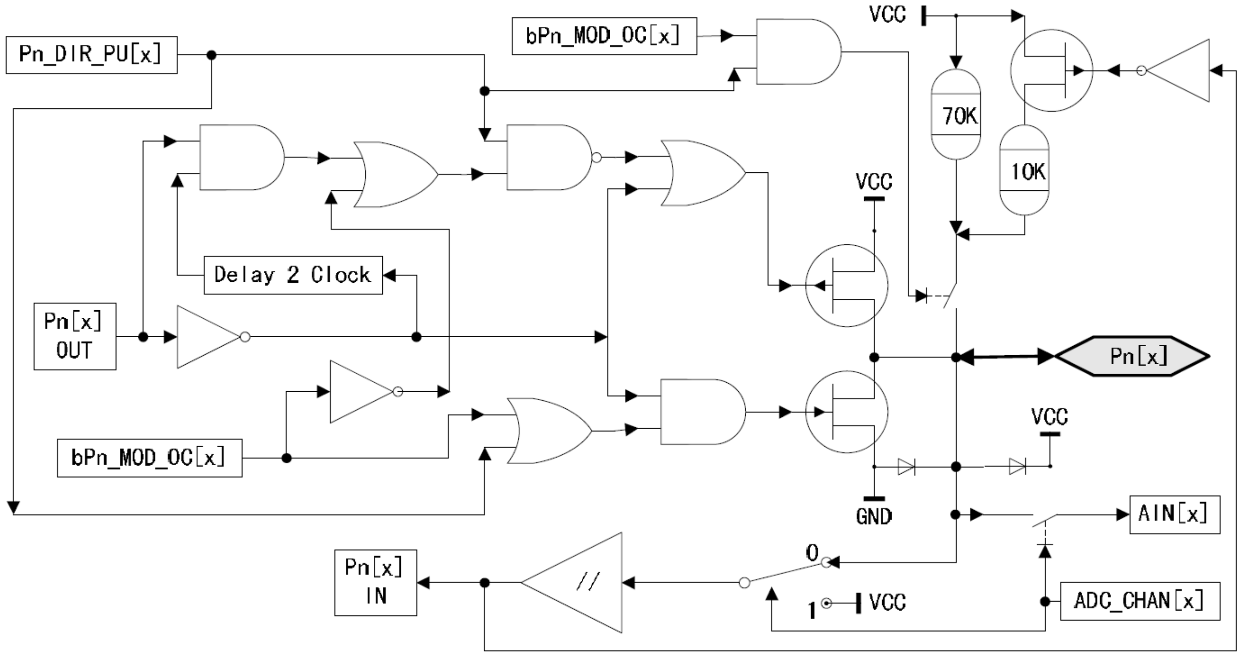
Pn_MOD_OC	Pn_DIR_PU	Working mode description
0	0	High resistance input mode, no pull-up resistance of pin
0	1	Push pull output mode, with symmetrical driving ability, can output or absorb large current
1	0	Open drain output, support high resistance input, no pull-up resistance pin
1	1	Quasi bidirectional mode (standard 8051), open drain output, support input, pin has pull-up resistance, when the output from low level to high level, automatically drive two clock cycles of high level to accelerate conversion

P1 and P3 ports support pure input or push-pull output and quasi bidirectional modes.Each pin has an internal pull-up resistor that can be controlled freely, as well as a protection diode connected to VCC and GND.

Figure 10.2.1 is the equivalent schematic diagram of P1. X pin of P1 port, which can be applied to P3 port after removing ain.After the VCC in the figure is changed to V33, it is applicable to P3.6 and P3.7, that is, the pull-up or input or output high level of P3.6 and P3.7 can only reach V33 voltage.

P3.6 and P3.7 can choose standard pull-up resistor (to V33), 15K Ω pull-down resistor, or provide 1.5k Ω strong pull-up resistor (to V33) for one of the pins.The standard pull-up resistor is only available in busb_IO_When en = 0, it is valid in GPIO mode, and is controlled by P3_DIR_Pu bit 7 bit 6 control; pull-down resistance in BUC_RESET_When Sie = 0, it is determined by baud_PD_Dis control, and busb_IO_1.5k Ω strong pull-up resistance is prior to pull-down resistance, and the resistance is independent of en_RESET_When Sie = 0, BUC_DEV_PU_EN control, and busb_IO_EN is irrelevant.

Figure 10.2.1 I / O pin equivalent schematic diagram



10.4 GPIO multiplexing and mapping

Some I / O pins of ch552 have multiplexing function. After power on, they are all general I / O pins by default. After enabling different function modules, corresponding pins are configured as function pins corresponding to their respective function modules.

Pin function selection register (pin_FUNC)：

position	name	visit	describe	reset value
7	bUSB_IO_EN	RW	USB UDP / UDM pin enable bit, if this bit is 0, P3.6 / P3.7 is used for GPIO and supports P3_DIR_Pu control pull-up resistor, support P3_MOD_OC; if this bit is 1, P3.6 / P3.7 is used for UDP / UDM and is controlled by USB module_DIR_Pu and P3_MOD_OC has no effect on it	1
6	bIO_INT_ACT	R0	GPIO interrupt request activation status: When Bie_IO_When edge = 0, the bit is 1, which indicates the GPIO input effective level, and the request will be interrupted. If the value is 0, it means the input invalid level; When Bie_IO_When edge = 1, this bit is used as	0

			the edge interrupt flag, and a value of 1 indicates that an effective edge is detected. This bit cannot be reset by software, and can only be used in reset or level	
			It is automatically cleared in break mode or when entering the corresponding interrupt service program	
5	bUART1_PIN_X	RW	Uart1 pin mapping enable bit, if this bit is 0, rxd1 / txd1 is used P1.6 / P1.7; if this bit is 1, then rxd1 / txd1 uses p3.4 / p3.2	0
4	bUART0_PIN_X	RW	UART0 pin mapping enable bit, if this bit is 0, rxd0 / txd0 is used P3.0 / P3.1; if this bit is 1, rxd0 / txd0 uses P1.2 / p1.3	0
3	bPWM2_PIN_X	RW	Pwm2 pin mapping enable bit, if this bit is 0, pwm2 uses p3.4; this bit is 1Then pwm2 uses P3.1	0
2	bPWM1_PIN_X	RW	Pwm1 pin mapping enable bit, if this bit is 0, pwm1 uses P1.5; this bit is 1Then pwm1 uses P3.0	0
1	bT2EX_PIN_X	RW	T2ex / CAP2 pin mapping enable bit, if this bit is 0, t2ex / CAP2 is used P1.1; if this bit is 1, then t2ex / CAP2 uses rst	0
0	bT2_PIN_X	RW	T2 / cap1 pin mapping enable bit, if this bit is 0, T2 / cap1 uses P1.0; if this bit is 1, T2 / cap1 uses P1.4	0

Table 10.4.1 list of GPIO pin multiplexing functions

GPIO	Other functions: from left to right
RST	RST、bT2EX_、bCAP2_、bRST
P1[0]	T2/bT2、CAP1/bCAP1、TIN0、P1.0
P1[1]	T2EX/bT2EX、CAP2/bCAP2、TIN1、VBUS2、AIN0、P1.1
P1[2]	XI、RXD_/bRXD_、P1.2
P1[3]	XO、TXD_/bTXD_、P1.3
P1[4]	T2_/bT2_、CAP1_/bCAP1_、SCS/bSCS、TIN2、UCC1、AIN1、P1.4
P1[5]	MOSI/bMOSI、PWM1/bPWM1、TIN3、UCC2、AIN2、P1.5
P1[6]	MISO/bMISO、RXD1/bRXD1、TIN4、P1.6
P1[7]	SCK/bSCK、TXD1/bTXD1、TIN5、P1.7
P3[0]	PWM1_/bPWM1_、RXD/bRXD、P3.0
P3[1]	PWM2_/bPWM2_、TXD/bTXD、P3.1
P3[2]	TXD1_/bTXD1_、INT0/bINT0、VBUS1、AIN3、P3.2
P3[3]	INT1/bINT1、P3.3
P3[4]	PWM2/bPWM2、RXD1_/bRXD1_、T0/bT0、P3.4

P3[5]	T1/bT1、P3.5
P3[6]	UDP/bUDP、P3.6
P3[7]	UDM/bUDM、P3.7

The priority from left to right mentioned in the above table refers to the priority when multiple function modules compete to use the GPIO.For example, when P3.1 is used for TXD serial transmission, P3.0 can still be used for higher priority pwm1 output.

11 External bus

Ch552 does not provide bus signal to the outside of the chip and does not support external bus, but can access the on-chip xram normally.

External bus auxiliary setting register (Xbus_AUX)：

position	name	visit	describe	reset value
7	bUART0_TX	R0	Indicates the sending status of UART0. A value of 1 indicates that it is in the process of sending	0
6	bUART0_RX	R0	Indicates the receiving status of UART0, 1 indicates receiving in progress	0
5	bSAFE_MOD_ACT	R0	Indicates the state of safe mode. A value of 1 indicates that it is currently in safe mode	0
4	retain	RO	retain	0
3	GF2	RW	General flag bit 2: the user can define it by himself, and can be reset or set by software	0
2	bDPTR_AUTO_INC	RW	Enable in MOVX_@After dptr instruction is completed, dptr will automatically add 1	0
1	retain	RO	retain	0
0	DPS	RW	Double dptr data pointer selection bit: when the bit is 0, select dptr0; if this bit is 1, select dptr1	0

12 Timer

12.1 Timer0/1

Timer0 / 1 is two 16 bit timers / counters. Timer0 and Timer1 are configured through TCON and tmod. TCON is used for start control, overflow interrupt and external interrupt control of timer / counter t0 and T1.Each timer is a 16 bit timing unit composed of two 8-bit registers.The high byte counter of timer 0 is Th0 and the low byte is tl0; the high byte counter of timer 1 is
Th1, the low byte is TL1.Timer 1 can also be used as baud rate generator of UART0.

Table 12.1.1 timer0 / 1 related register list

name	address	describe	reset value
TH1	8Dh	Timer1 count high byte	Xxh
TH0	8Ch	Timer0 counts high bytes	Xxh
TL1	8Bh	Timer1 counts low bytes	Xxh
TL0	8Ah	Timer0 counts low bytes	Xxh

TMOD	89h	Timer0 / 1 mode register	00h
TCON	88H	Timer0 / 1 control register	00h

Timer / counter 0 / 1 control register (TCON)

position	name	visit	describe	reset value
7	TF1	RW	Timer1 overflows the interrupt flag bit, and it will be cleared automatically after entering timer 1 interrupt	0
6	TR1	RW	Timer1 start / stop bit, set 1 to start, set or reset by software	0
5	TF0	RW	Timer0 overflows the interrupt flag bit and is automatically cleared after entering timer 0 interrupt	0
4	TR0	RW	Timer 0 start / stop bit, set 1 to start, set or reset by software	0
3	IE1	RW	The interrupt request flag bit of INT1 external interrupt 1 is cleared automatically after entering the interrupt	0
2	IT1	RW	INT1 external interrupt 1 trigger mode control bit, this bit is 0 to select external interrupt as low level trigger; this bit is 1 to select external interrupt as falling edge trigger	0
1	IE0	RW	The interrupt request flag bit of INT0 external interrupt 0 is cleared automatically after entering the interrupt	0
0	IT0	RW	INT0 external interrupt 0 trigger mode control bit, this bit is 0 to select external interrupt as low level trigger; this bit is 1 to select external interrupt as falling edge trigger	0

Timer / counter 0 / 1 mode register (tmod)

position	name	visit	describe	reset value
7	bT1_GATE	RW	The gate enable bit controls whether the timer 1 start is affected by the external interrupt signal INT1.If this bit is 0, whether timing / counter 1 is started or not is independent of INT1; if this bit is 1, it can be started only when INT1 pin is high and Tr1 is 1	0
6	bT1_CT	RW	Timing or counting mode selection bit, the bit 0 works in timing mode; the bit 1 works in counting mode, and uses the falling edge of T1 pin as the clock	0
5	bT1_M1	RW	Timing / counter 1 mode selection high	0
4	bT1_M0	RW	Timer / counter 1 mode selection low	0
3	bT0_GATE	RW	The gate enable bit controls whether the timer 0 start is affected by the external interrupt signal INT0.If this bit is 0, whether timing / counter 0 is	0

			started or not has nothing to do with INT0; if this bit is 1, it can be started only when INT0 pin is high and tr0 is 1	
2	bT0_CT	RW	Select bit for timing or counting mode, the bit is 0 working in timing mode; this bit is 1 working in counting mode, and the falling edge of t0 pin is used as clock	0
1	bT0_M1	RW	Timing / counter 0 mode selection high	0
0	bT0_M0	RW	Timer / counter 0 mode selection low	0

Table 12.1.2 BTN_M1 and BTN_M0 selects timern working mode (n = 0, 1)

bTn_M1	bTn_M0	Timern working mode (n = 0,1)
0	0	Mode 0: 13 bit timing / counter n, the counting unit is composed of the lower 5 bits of TLN and thn, and the upper 3 bits of TLN are invalid.When the count changes from 13 bits all 1 to all 0, the overflow flag TFN is set and the initial value needs to be reset
0	1	Mode 1: 16 bit timing / counter n, the counting unit is composed of TLN and thn.When the count changes from 16 bit all 1 to all 0, the overflow flag TFN is set and the initial value needs to be reset
1	0	Mode 2: 8-bit overload timer / counter n, the counting unit uses TLN and thn as overload counting unit. When the count changes from 8 bits all 1 to all 0, the overflow flag TFN is set and the initial value is automatically loaded from thn
1	1	Mode 3: in case of timer / counter 0, timer / counter 0 is divided into two parts tl0 and Th0, Tl0 is used as an 8-bit timer / counter, occupying all control bits of timer0; Th0 is also used as another 8-bit timer, occupying the Tr1, TF1 and interrupt resources of Timer1. At this time, Timer1 is still available, but the start control bit Tr1 and overflow flag bit TF1 cannot be used. If it is timer / counter 1, entering mode 3 will stop timer / counter 1.

Timern count low byte (TLN) (n = 0, 1): 0

position	name	visit	describe	reset value
[7:0]	TLn	RW	Timern counts low bytes	Xxh

Timern count high byte (thn) (n = 0, 1)

position	name	visit	describe	reset value
[7:0]	THn	RW	Timern counts high bytes	Xxh

12.2 Timer2

Timer2 is a 16 bit automatic overload timer / counter, which is configured through t2con and t2mod registers. The high byte counter of timer 2 is Th2, and the low byte is TL2.In addition, it can capture the signal level of CAP2 in the rtua2, which can be used as the capture rate of CAP2.

Table 12.2.1 timer2 related register list

name	address	describe	reset value
TH2	CDh	Timer2 counter high byte	00h
TL2	CCh	Timer2 counter low byte	00h
T2COUNT	CCh	TL2 and Th2 constitute a 16 bit SFR	0000h
T2CAP1H	CFh	Timer2 captures 1 data high byte (read only)	Xxh
T2CAP1L	CEh	Timer2 capture 1 data low byte (read only)	Xxh
T2CAP1	CEh	T2cap1l and t2cap1h constitute a 16 bit SFR	xxxxh
RCAP2H	CBh	Count overload / capture 2 data register high byte	00h
RCAP2L	CAh	Count overload / capture 2 data register low byte	00h
RCAP2	CAh	Rcap2l and rcap2h constitute a 16 bit SFR	0000h
T2MOD	C9h	Timer2 mode register	00h
T2CON	C8h	Timer2 control register	00h

Timer / counter 2 control register (t2con)

position	name	visit	describe	reset value
7	TF2	RW	When BT2_CAP1_When en = 0, it is the overflow interrupt flag of timer2. When the timer 2 count changes from all 16 bits of 1 to all 0, the overflow flag is set to 1 and the software is required to reset. When rCLK = 1 or TCLK = 1, this bit will not be set to 1	0
7	CAP1F	RW	When BT2_CAP1_When en = 1, timer 2 captures 1 interrupt flag, which is triggered by effective edge of T2, and needs to be reset by software	0
6	EXF2	RW	When exen2 = 1, the external trigger flag of timer2 is set to 1 by the effective edge trigger of t2ex, which needs to be reset by software	0
5	RCLK	RW	UART0 receive clock selection, the bit is 0 to select Timer1 overflow pulse to generate baud rate; this bit is 1 to select timer2 overflow pulse to generate baud rate	0
4	TCLK	RW	UART0 transmission clock selection, this bit is 0 to select Timer1 overflow pulse to generate baud rate; this bit is 1 to select timer2 overflow pulse to generate baud rate	0
3	EXEN2	RW	T2ex trigger enable bit, this bit is 0, ignore t2ex; this bit is 1 enable triggering overload or capture when t2ex is effective edge	0
2	TR2	RW	Timer 2 start / stop bit, set 1 to start, set or reset by software	0
1	C_T2	RW	Timer2 clock source selection bit, which is 0 uses the internal clock; the bit 1 uses the edge count	0

			based on the falling edge of T2 pin	
0	CP_RL2	RW	Timer2 function selects bit. If rCLK or TCLK is 1, this bit should be forced to 0.If this bit is 0, timer2 is used as timer / counter, and the initial value can be overloaded automatically when the counter overflows or the level of t2ex changes; if this bit is 1, the capture 2 function of timer2 can be enabled to capture the effective edge of t2ex	0

Timer / counter 2 mode register (t2mod)

<table>
<tr><th>position</th><th>name</th><th>visit</th><th colspan="2">describe</th><th>reset value</th></tr>
<tr><td>7</td><td>bTMR_CLK</td><td>RW</td><td colspan="2">The fastest clock mode of t0 / T1 / T2 timer with fast clock selected is enabled. If the bit is 1, the system main frequency Fsys without frequency division is used as the counting clock; if the bit is 0, the frequency division clock is used.This bit has no effect on the timer that selects the standard clock</td><td>0</td></tr>
<tr><td>6</td><td>bT2_CLK</td><td>RW</td><td colspan="2">The internal clock frequency selection bit of timer2: if the bit is 0, the standard clock is selected, the timing / counting mode is Fsys / 12, and the UART0 clock mode is Fsys / 4; this bit is 1 to select the fast clock, and the timing / counting mode is Fsys / 4 (BTMR)_CLK = 0) or Fsys(bTMR_CLK = 1), UART0 clock mode is Fsys / 2 (BTMR)_CLK = 0) or Fsys (BTMR)_CLK=1)</td><td>0</td></tr>
<tr><td>5</td><td>bT1_CLK</td><td>RW</td><td colspan="2">Timer 1 internal clock frequency selection bit, the bit is 0, select the standard clock Fsys / 12; Select fast clock Fsys / 4 (BTMR) for 1_CLK = 0) or Fsys (BTMR)_CLK=1)</td><td>0</td></tr>
<tr><td>4</td><td>bT0_CLK</td><td>RW</td><td colspan="2">The internal clock frequency selection bit of timer0, which is 0, selects the standard clock Fsys / 12;
Select fast clock Fsys / 4 (BTMR) for 1_CLK = 0) or Fsys (BTMR)_CLK=1)</td><td>0</td></tr>
<tr><td>3</td><td>bT2_CAP_M1</td><td>RW</td><td>Timer2 capture mode high bit</td><td rowspan="2">Capture mode selection:
X0: from falling edge to falling edge
01: from any edge to any edge, that is, the level changes
11: from rising edge to rising edge</td><td>0</td></tr>
<tr><td>2</td><td>bT2_CAP_M0</td><td>RW</td><td>Timer2 capture mode low bit</td><td>0</td></tr>
<tr><td>1</td><td>T2OE</td><td>RW</td><td colspan="2">Timer2 clock output enable bit, which is 0 disable output; this bit is 1 enable
T2 pin output clock, the frequency is half of the overflow rate of timer2</td><td>0</td></tr>
<tr><td>0</td><td>bT2_CAP1_EN</td><td>RW</td><td colspan="2">When rCLK = 0, TCLK = 0, CP_RL2=1、C_When T2 = 0 and t2oe = 0, the capture 1 mode is</td><td>0</td></tr>
</table>

			enabled, and this bit is 1 to enable the capture 1 function to capture the effective edge of T2; when the bit is 0, the capture 1 is disabled	

Count overload / capture 2 data register (rcap2)

position	name	visit	describe	reset value
[7:0]	RCAP2H	RW	High byte of overloaded value in timer / counter mode; high byte in capture mode High byte of timer captured by CAP2	00h
[7:0]	RCAP2L	RW	It is the low byte of the overloaded value in timer / counter mode; it is in capture mode Low byte of timer captured by CAP2	00h

Timer2 counter (t2count)

position	name	visit	describe	reset value
[7:0]	TH2	RW	Current counter high byte	00h
[7:0]	TL2	RW	Current counter low byte	00h

Timer2 capture 1 data (t2cap1)

position	name	visit	describe	reset value
[7:0]	T2CAP1H	RO	High byte of timer captured by cap1	Xxh
[7:0]	T2CAP1L	RO	Low byte of timer captured by cap1	Xxh

12.3 PWM function

Ch552 provides two-way 8-bit PWM. PWM can choose the default output polarity as low-level or high-level, and can dynamically modify the output duty cycle of PWM. After integrating low-pass filter with simple RC resistor and capacitor, various output voltages can be obtained, which is equivalent to low-speed DAC.

Pwm1 output duty cycle = PWM_Data1 / 256, support range 0% to 99.6%.

Pwm2 output duty cycle = PWM_Data2 / 256, support range 0% to 99.6%.In practical application, it is recommended to allow PWM pin output and set PWM output pin as push-pull output mode.

12.3.1 pwm1 and pwm2

Table 12.3.1 pwm1 and pwm2 related register list

name	address	describe	reset value
PWM_CK_SE	9Eh	PWM clock frequency division setting register	00h
PWM_CTRL	9Dh	PWM Control Register	02h
PWM_DATA1	9Ch	Pwm1 data register	Xxh

PWM_DATA2	9Bh	Pwm2 data register	Xxh

Pwm2 data register (PWM_DATA2):

position	name	visit	describe	reset value
[7:0]	PWM_DATA2	RW	Store pwm2 current data, Duty cycle of pwm2 output active level = PWM_DATA2/256	Xxh

Pwm1 data register (PWM_DATA1):

position	name	visit	describe	reset value
[7:0]	PWM_DATA1	RW	Store pwm1 current data, Duty cycle of pwm1 output active level = PWM_DATA1/256	Xxh

PWM control register (PWM_CTRL):

position	name	visit	describe	reset value
7	bPWM_IE_END	RW	This bit is 1 to enable the end of PWM cycle or MFM buffer air break	0
6	bPWM2_POLAR	RW	Control the output polarity of pwm2. If the bit is 0, the low level is default and the high level is valid; if the bit is 1, the default high level and low level are valid	0
5	bPWM1_POLAR	RW	Control the output polarity of pwm1. If this bit is 0, the default low level and high level are valid; if this bit is 1, the default high level and low level are valid	0
4	bPWM_IF_END	RW	PWM cycle end interrupt flag bit, this bit is 1 to indicate interrupt, write 1Reset or reload PWM_Clear data1 data	0
3	bPWM2_OUT_EN	RW	Pwm2 output enable, this bit is 1 enable pwm2 output	0
2	bPWM1_OUT_EN	RW	Pwm1 output enable, this bit is 1 enable pwm1 output	0
1	bPWM_CLR_ALL	RW	This bit is 1 to clear pwm1 and pwm2 count and FIFO, and software reset is required	1
0	retain	RO	retain	0

PWM clock frequency division setting register (PWM_CK_SE):

position	name	visit	describe	reset value
[7:0]	PWM_CK_S	RW	Setting PWM clock division divisor	00h

	E			

12.4 timer function

12.4.1 Timer0/1

(1) Set t2mod to select timer internal clock frequency, if BTN_If CLK (n = 0 / 1) is 0, the clock corresponding to timer0 / 1 is Fsys / 12; if BTN_If CLK is 1, then BTMR_CLK = 0 or 1, select Fsys / 4 or Fsys as the clock.

(2) Set tmod to configure timer working mode.

模式 0：13 位定时/计数器

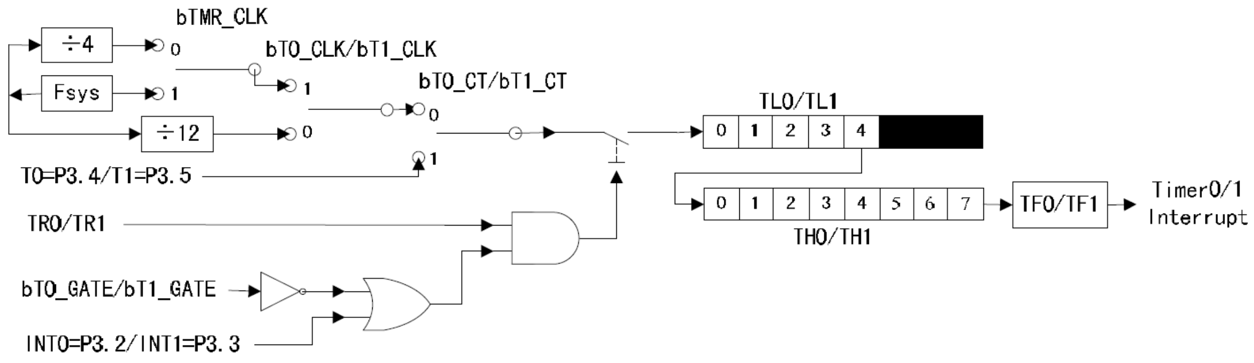
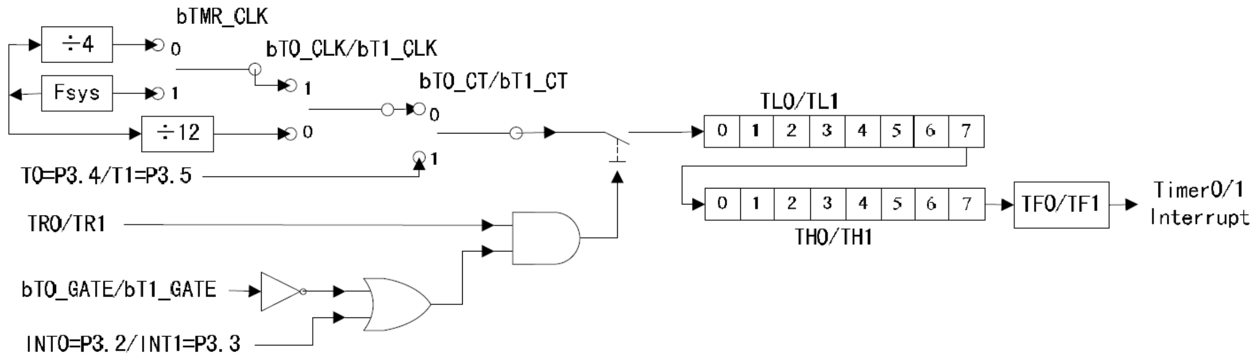


Figure 12.4.1.1 timer0 / 1 mode 0

模式 1：16 位定时/计数器



模式 2：自动重载 8 位定时/计数器

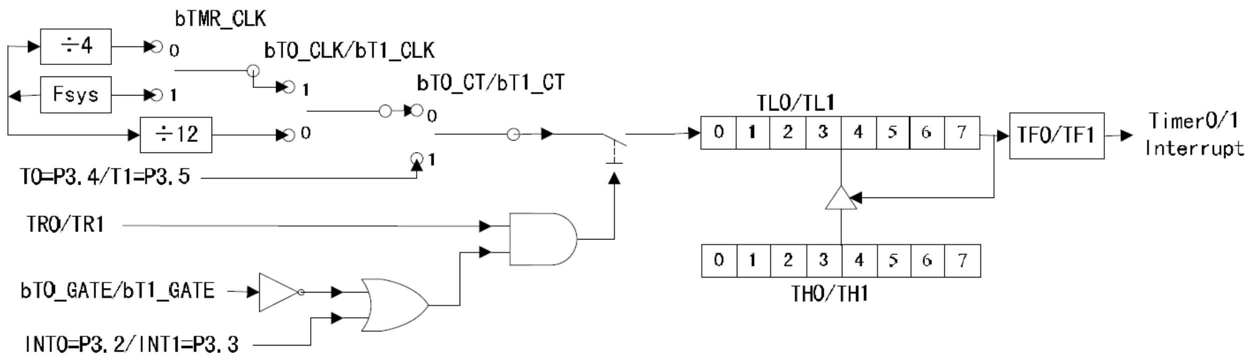
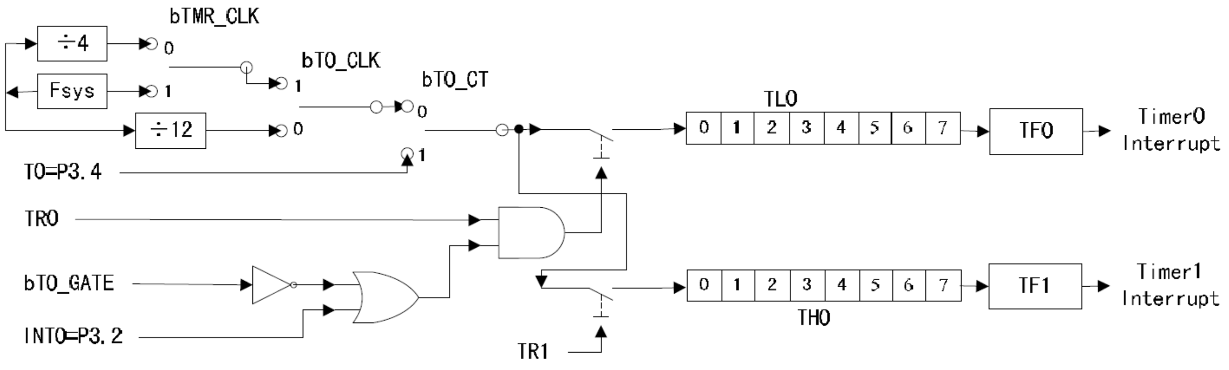


Figure 12.4.1.3 timer0 / 1 mode 2

Mode 3: timer0 is decomposed into two independent 8-bit timers / counters, and the Tr1 control bit of Timer1 is used

If mode 3 is started instead of the borrowed Tr1 control bit, Timer1 will stop running when Timer1 enters mode 3.

模式 3：Timer0 分解为两个独立的 8 位定时/计数器，并借用 Timer1 的 TR1 控制位；Timer1 通过是否启动模式 3 代替被借用的 TR1 控制位，Timer1 进入模式 3 则 Timer1 停止运行。



(3) Set the initial value TLN and thn of timer / counter (n = 0 / 1).
(4) Set the bit TRN (n = 0 / 1) in TCON to start or stop the timer / counter, which can be queried by bit TFN (n = 0 / 1) or detected by interrupt mode.

12.4.2 Timer2
Timer2 16 bit overload timer / counter mode:
(1) Set the bit rCLK and TCLK in t2con to 0, and select the non serial baud rate generator mode.
(2) Set bit C in t2con_If T2 is 0, select to use the internal clock and turn to step (3); or set 1 to select the falling edge of T2 pin as the counting clock and skip step (3).
(3) Set t2mod to select timer internal clock frequency, if BT2_If the clock frbk is 12, then_If CLK is 1, then BTMR_CLK = 0 or 1, select Fsys / 4 or Fsys as the clock.
(4) Set the bit CP of t2con_When RL2 is 0, select the 16 bit overload timer / counter function of timer2.
(5) Set rcap2l and rcap2h as the overload value after timer overflow, and set TL2 and Th2 as the initial value of timer
Rcap2l is the same as rcap2h), TR2 is set to 1, and timer2 is enabled.
(6) The current timer / counter status can be obtained by querying the interrupt of the timer 2 or by querying the state of the timer 2.

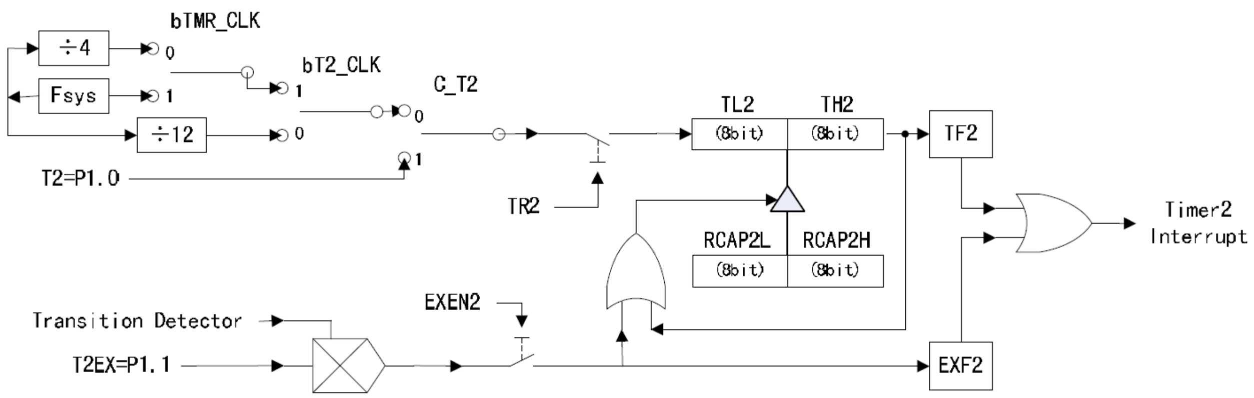


图 12.4.2.1 Timer2 16 位重载定时/计数器

Timer2 clock output mode:

Refer to 16 bit overload timer / counter mode and set bit t2oe in t2mod to 1, then output from T2 pin is enabled
Two division clock of the frequency.

Timer 2 serial port 0 baud rate generator mode:
(1) Set bit C in t2con_If T2 is 0, select the internal clock, or set 1 to select the falling edge of T2 pin as the clock. Set the bit rCLK and TCLK in t2con as 1 or one of them as 1 as required to select the serial port baud rate generator mode.
(2) Set t2mod to select timer internal clock frequency, if BT2_If CLK is 0, the clock of timer2 is Fsys / 4; if BT2_If CLK is 1, then BTMR_CLK = 0 or 1, select Fsys / 2 or Fsys as the clock.
(3) Set rcap2l and rcap2h as overload values after timer overflow, set TR2 to 1, and turn on timer2.

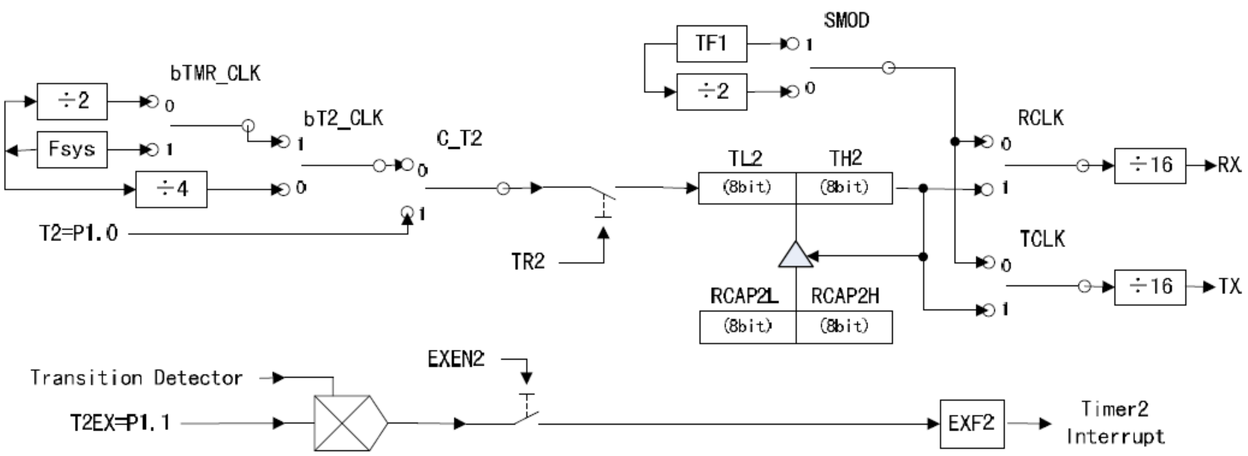


图 12.4.2.2 Timer2 UART0 波特率发生器

Timer2 dual channel capture mode:
(1) Set the bit rCLK and TCLK in t2con to 0, and select the non serial baud rate generator mode.
(2) Set bit C in t2con_If T2 is 0, select to use the internal clock and turn to step (3); or set 1 to select the falling edge of T2 pin as the counting clock and skip step (3).
(3) Set t2mod to select timer internal clock frequency, if BT2_If CLK is 0, the clock of timer2 is Fsys / 12; if BT2_If CLK is 1, then BTMR_CLK = 0 or 1, select Fsys / 4 or Fsys as the clock.
(4) Set bit BT2 of t2mod_CAP_M1 and BT2_CAP_M0 selects the corresponding edge capture mode.
(5) Set the bit CP of t2con_When RL2 is 1, select the capture function of timer2 to t2ex pin.
(6) Set TL2 and Th2 as the initial values of the timer, set TR2 to 1, and turn on timer2.
(7) When CAP2 capture is completed, rcap2l and rcap2h will save the count values of TL2 and Th2 at that time, and set exf2 to generate interrupt. The difference between rcap2l and rcap2h captured next time and rcap2l and rcap2h captured last time is the signal width between the two effective edges.
(8) If bit C in t2con_T2 is 0, and bit BT2 in t2mod_CAP1_If en is 1, the capture function of timer2 to T2 pin will be enabled at the same time. When cap1 capture is completed, t2cap1l and t2cap1h will save the count values of TL2 and Th2 at that time, and set cap1f to generate interrupt.

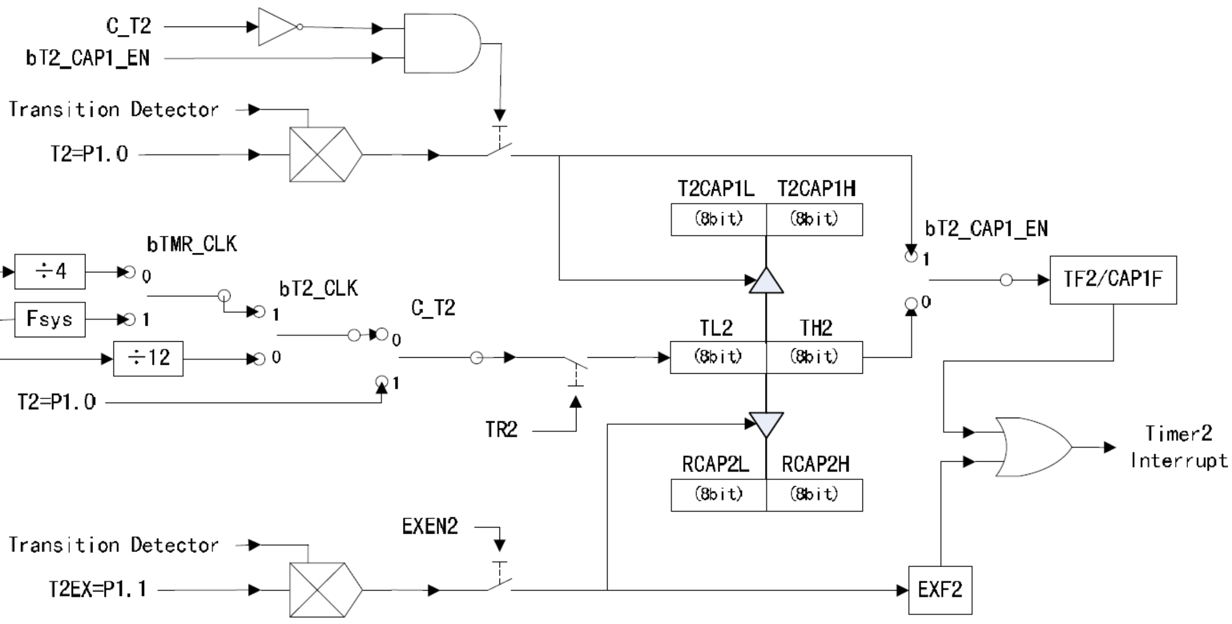


图 12.4.2.3 Timer2 捕捉模式

13UART (universal asynchronous transceiver)

13.1 introduction to UART

Ch552 chip provides two full duplex asynchronous serial ports: UART0 and uart1.Ch551 only provides UART0.

UART0 is a standard MCS51 serial port, and its data receiving and sending are realized by SBUF accessing physically separate receive / transmit registers.The data written to SBUF is loaded into the transmit register, and the read operation of SBUF corresponds to the receive buffer register.

Uart1 is a simplified MCS51 serial port, and its data receiving and sending are realized by sbuf1 accessing physically separate receive / transmit registers.The data written to sbuf1 is loaded into the transmit register, and the read operation of sbuf1 corresponds to the receive buffer register.Uart1 comparison UART0 eliminates the multi machine communication mode and fixed baud rate, and uart1 has an independent baud rate generator.

13.2 UART register table 13.2.1 list of UART related registers

name	address	describe	reset value
SCON	98H	UART0 control register	00h
SBUF	99H	UART0 data register	Xxh
SCON1	C0h	Uart1 control register	40H
SBUF1	C1h	Uart1 data register	Xxh
SBAUD1	C2h	Uart1 baud rate setting register	Xxh

13.2.1 UART0 register description UART0 control register (scon)

position	name	visit	describe	reset value
7	SM0	RW	Bit 0 is selected for UART0 working mode, and 8-bit data asynchronous communication is selected when the bit is 0 1Select 9-bit data asynchronous communication	0
6	SM1	RW	UART0 working mode selection bit 1, this bit is 0 to set the fixed baud rate; this bit is 1 to set the variable baud rate, which is generated by timer T1 or T2	0
5	SM2	RW	UART0 multi machine communication control bit: when receiving data in mode 2 and 3, when SM2 = 1, if rb8 is 0, then RI is not set to 1, and reception is invalid; if rb8 is 1, then RI is set to 1, and reception is effective; when SM2 = 0In mode 1, if SM2 = 1, the receive is valid only when a valid stop bit is received; in mode 0, the SM2 bit must be set to 0	0
4	REN	RW	UART0 is allowed to receive the control bit, which is 0 to prohibit receiving; the bit is 1 to allow receiving	0
3	TB8	RW	In mode 2 and 3, TB8 is used to write the 9th bit of transmitted data, which can be parity bit; in multi machine communication, it is used to indicate whether the host sends address byte or data byte, with TB8 = 0 as data and TB8 = 1 as address	0
2	RB8	RW	In mode 1, if SM2 = 0, rb8 is used to store the received stop bit; in mode 0, rb8 is not used	0
1	TI	RW	Send interrupt flag bit, a data byte after sending is set by hardware, need software reset	0
0	RI	RW	Receive interrupt flag bit. After a data byte is received, it is set by hardware and needs to be reset by software	0

Table 13.2.1.1 UART0 mode selection

SM 0	SM 1	describe
0	0	Mode 0, shift register mode, baud rate fixed is Fsys / 12
0	1	Mode 1, 8-bit asynchronous communication mode, variable baud rate, generated by timer T1 or T2
1	0	Mode 2, 9-bit asynchronous communication mode, baud rate is Fsys / 128 (SMOD = 0) or Fsys / 32 (SMOD = 1)
1	1	Mode 3, 9-bit asynchronous communication mode, variable baud rate, generated by timer T1 or T2

In modes 1 and 3, the UART0 baud rate is generated by timer T1 when rCLK = 0 and TCLK = 0.T1 should be set to Mode 2 auto overload 8-bit timer mode, BT1_CT and BT1_Gate must all be 0, divided into the following types of clock conditions.

Table 13.2.1.2 calculation formula of UART0 baud rate generated by T1

bTMR_CL	bT1_CL	SMOD	describe

K	K		
1	1	0	Th1 = 256 - Fsys / 32 / baud rate
1	1	1	Th1 = 256 - Fsys / 16 / baud rate
0	1	0	Th1 = 256 - Fsys / 4 / 32 / baud rate
0	1	1	Th1 = 256 - Fsys / 4 / 16 / baud rate
X	0	0	Th1 = 256 - Fsys / 12 / 32 / baud rate
X	0	1	Th1 = 256 - Fsys / 12 / 16 / baud rate

In modes 1 and 3, the UART0 baud rate is generated by timer T2 when rCLK = 1 or TCLK = 1.T2 should be set to 16 bit automatic overload baud rate generator mode, C_T2 and CP_RL2 must all be 0, divided into the following types of clock conditions.Table 13.2.1.3 calculation formula of UART0 baud rate generated by T2

bTMR_CLK	bT2_CLK	describe
1	1	Rcap2 = 65536 - Fsys / 16 / baud rate
0	1	Rcap2 = 65536 - Fsys / 2 / 16 / baud rate
X	0	Rcap2 = 65536 - Fsys / 4 / 16 / baud rate

UART0 data register (SBUF)

position	name	visit	describe	reset value
[7:0]	SBUF	RW	UART0 data register includes two physical separate registers: transmit register and receive register.Writing data to SBUF corresponds to sending data register; reading data from SBUF corresponds to receiving data register	Xxh

13.2.2 uart1 register description

Uart1 control register (scon1)

position	name	visit	describe	reset value
7	U1SM0	RW	Uart1 working mode selection bit, the bit 0 selects 8-bit data asynchronous communication; the bit 1 selects 9-bit data asynchronous communication	0
6	retain	RO	retain	1
5	U1SMOD	RW	Select the baud rate of uart1: 0-slow mode; 1-fast mode	0
4	U1REN	RW	Uart1 allows receiving control bit, which is 0 to prohibit receiving; this bit is 1 to allow receiving	0
3	U1TB8	RW	Bit 9 of the transmitted data. In the 9-bit data mode, TB8 is used to write the 9th bit of the transmitted data 9Bit, can be parity bit; in 8-bit data mode, TB8 ignores	0
2	U1RB8	RW	The 9th bit of the received data. In the 9-bit data mode, rb8 is used to store the 9th bit of the received	0

			data 9Bit; in 8-bit data mode, rb8 is used to store the received stop bits	
1	U1TI	RW	Send interrupt flag bit, a data byte after sending is set by hardware, need software reset	0
0	U1RI	RW	Receive interrupt flag bit. After a data byte is received, it is set by hardware and needs to be reset by software	0

Uart1 baud rate is generated by sbaud1 setting. According to u1smod selection, it can be divided into two situations: when u1smod = 0, sbaud1 = 256 - Fsys / 32 / baud rate; when u1smod = 1, sbaud1 = 256 - Fsys / 16 / baud rate.

Uart1 data register (sbuf1)

position	name	visit	describe	reset value
[7:0]	SBUF1	RW	Uart1 data register includes two physical separate registers: transmit register and receive register.Writing data to sbuf1 corresponds to sending data register; reading data from sbuf1 corresponds to receiving data register	Xxh

13.3 UART application

UART0 application:
(1) Select baud rate generator of UART0, select timer T1 or T2, and configure corresponding counter.
(2) Turn on timer T1 or T2.
(3) Set SM0, SM1 and SM2 of scon, and select the working mode of serial port 0.Set Ren to 1 to enable UART0 reception.
(4) Can set serial port interrupt or query RI and Ti interrupt status.
(5) Read and write SBUF to realize serial data receiving and sending, and the allowable baud rate error of serial port receiving signal is not more than 2%.

Uart1 application:
(1) Select u1smod and set sbaud1 according to baud rate.
(2) Set u1sm0 of scon1 and select the working mode of serial port 1.Set u1ren to 1 to enable uart1 reception.
(3) Can set serial port 1 interrupt or query u1ri and u1ti interrupt status.
(4) Read and write sbuf1 to realize serial port 1 data receiving and sending, and the allowable baud rate error of serial port receiving signal is not more than 2%.

14Synchronous serial interface SPI

14.1 introduction to SPI

The chip ch552 provides SPI interface for high-speed synchronous data transmission with peripherals.
(1) Support master mode and slave mode;
(2) Mode 0 and mode 3 clock modes are supported;
(3) 3-wire full duplex or 2-wire half duplex mode can be selected;

(4) . select MSB high bit first send or LSB low bit send first;
(5) The clock frequency is adjustable, up to nearly half of the main frequency of the system;
(6) 1-byte receive FIFO and 1-byte transmit FIFO are built-in;
(7) In slave mode, it supports the first byte pre loading data, which is convenient for the host to get the returned data in the first byte immediately.

14.2 SPI register

Table 14.2.1 list of SPI related registers

name	address	describe	reset value
SPI0_SETUP	FCh	Spi0 setting register	00h
SPI0_S_PRE	FBh	Spi0 slave mode preset data register	20h
SPI0_CK_SE	FBh	Spi0 clock frequency division setting register	20h
SPI0_CTRL	FAh	Spi0 control register	02h
SPI0_DATA	F9h	Spi0 data transceiver register	Xxh
SPI0_STAT	F8h	Spi0 status register	08h

Spi0 setting register (spi0_SETUP)：

position	name	visit	describe	reset value
7	bS0_MODE_SLV	RW	Spi0 master slave mode selection bit. If this bit is 0, spi0 is master mode; if this bit is 1, spi0 is slave mode / device mode	0
6	bS0_IE_FIFO_OV	RW	In slave mode, FIFO overflow interrupt enable bit, which is 1 enable FIFO overflow interrupt; if this bit is 0, FIFO overflow does not generate interrupt	0
5	bS0_IE_FIRST	RW	When receiving the first byte completion interrupt enable bit in slave mode, if the bit is 1, the interrupt will be triggered when the first data byte is received in slave mode; if the bit is 0, no interrupt will be generated when the first byte is received	0
4	bS0_IE_BYTE	RW	Data byte transfer completion interrupt enable bit, which is 1, allows byte transfer completion interrupt; if this bit is 0, byte transfer completion does not generate interrupt	0
3	bS0_BIT_ORDER	RW	The bit sequence control bit of a data byte. If the bit is 0, the high bit of MSB is first; if the bit is 1, the low bit of LSB is first	0
2	retain	RO	retain	0
1	bS0_SLV_SELT	R0	In slave mode, if the bit is 0, it means that it is not currently selected; if the bit is 1, it means that it is currently in the selected state	0
0	bS0_SLV_PRELO	R0	In slave mode, the pre load data status bit,	0

	AD		which is 1, indicates that it is in the preload state after the slice selection is valid and before the data has been transmitted	

Spi0 clock frequency division setting register (spi0_CK_SE)：

position	name	visit	describe	reset value
[7:0]	SPI0_CK_SE	RW	Setting spi0 clock frequency division coefficient in host mode	20h

Spi0 slave mode preset data register (spi0_S_PRE)：

position	name	visit	describe	reset value
[7:0]	SPI0_S_PRE	RW	First transfer data in pre loaded slave mode	20h

Spi0 control register (spi0_CTRL)：

position	name	visit	describe	reset value
7	bS0_MISO_OE	RW	The miso output enable control bit of spi0, which is 1 to allow output, and 0 to disable output	0
6	bS0_MOSI_OE	RW	The MoSi output enable control bit of spi0, which is 1 to allow output and 0 to disable output	0
5	bS0_SCK_OE	RW	Spi0 SCK output enable control bit, this bit is 1 allowed output; this bit is 0 inhibit output	0
4	bS0_DATA_DIR	RW	Spi0 data direction control bit. If this bit is 0, the data will be output and only write FIFO as effective operation to start SPI transmission; if this bit is 1, input data, write or read FIFO will be regarded as effective operation to start SPI transmission	0
3	bS0_MST_CLK	RW	Spi0 host clock mode control bit, if this bit is 0, mode 0, the default low level of SCK is idle; if this bit is 1, mode 3, SCK default high level	0
2	bS0_2_WIRE	RW	If the mode of mosso is 2 and half duplex, the mode includes half line	0
1	bS0_CLR_ALL	RW	This bit is 1 to clear spi0 interrupt flag and FIFO, which needs software reset	1
0	bS0_AUTO_IF	RW	Enable bit that allows automatic clearing byte receiving completion interrupt flag through FIFO effective operation. If this bit is 1, it will automatically clear zero byte receiving completion interrupt flag S0 during FIFO effective read and write operation_IF_BYTE	0

Spi0 data transceiver register (spi0_DATA):

position	name	visit	describe	reset value
[7:0]	SPI0_DATA	RW	It includes two separate FIFOs: transmit and receive, read corresponds to receive data FIFO, write corresponds to transmit data FIFO, effective read and write operation	Xxh
			可以启动一次SPI 传输	

Spi0 status register (spi0_STAT):

position	name	visit	describe	reset value
7	S0_FST_ACT	R0	If this bit is 1, it means that the current status is completed when receiving the first byte in slave mode	0
6	S0_IF_OV	RW	In slave mode, FIFO overflow flag bit, 1 indicates FIFO overflow interrupt; 0 indicates no interrupt.Clear direct bit access or write 1 to clear.When bs0_DATA_When dir = 0, the interrupt is triggered by sending FIFO null; when bs0_DATA_When dir = 1, receive FIFO full trigger interrupt	0
5	S0_IF_FIRST	RW	In slave mode, the first byte completion interrupt flag bit is received. If this bit is 1, the first byte is received.Clear direct bit access or write 1	0
4	S0_IF_BYTE	RW	Data byte transfer completion interrupt flag bit. If this bit is 1, it indicates that a byte transfer is completed.Direct bit access reset or write 1 clear, or in bs0_AUTO_If = 1, clear through FIFO effective operation	0
3	S0_FREE	R0	The spi0 idle flag bit, which is 1, indicates that there is no SPI shift at present, which is usually in the neutral period between data bytes	1
2	S0_T_FIFO	R0	Spi0 sends FIFO count, valid value is 0 or 1	0
1	retain	R0	retain	0
0	S0_R_FIFO	R0	Spi0 receive FIFO count, valid value is 0 or 1	0

14.3 SPI transmission format

SPI host mode supports mode 0 and mode 3 transmission formats. SPI control register spin can be set_Bit BSN in Ctrl_MST_For CLK selection, ch552 always samples miso data at the rising edge of CLK.The data transmission format is shown in the figure below.

Mode 0: BSN_MST_CLK = 0

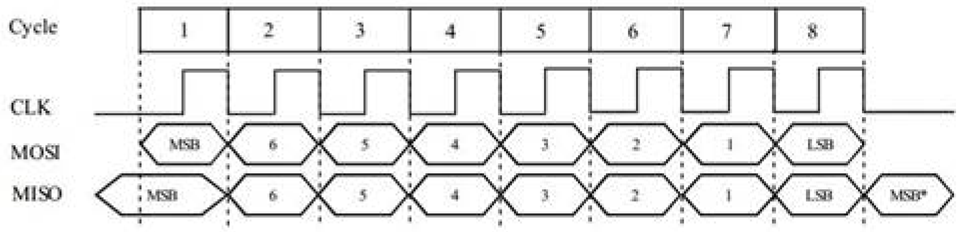


Figure 14.3.1 SPI mode 0 sequence diagram

Mode 3: BSN_MST_CLK = 1

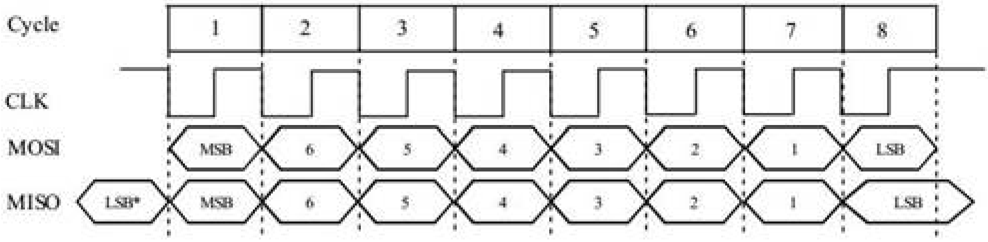


Figure 14.3.2 SPI mode 3 sequence diagram

14.4 SPI configuration

14.4.1 SPI host mode configuration

In SPI host mode, SCK pin outputs serial clock, and chip output pin can be specified as any I / O pin.

Spi0 configuration steps:

(1) Set SPI clock frequency division setting register spi0_CK_Se, configure SPI clock frequency.

(2) , set SPI setting register spi0_Bit bs0 of setup_MODE_SLV is 0 and configured as host mode.

(3) Set SPI control register spi0_Bit bs0 of Ctrl_MST_CLK, set to mode 0 or 3 as required.

(4) Set SPI control register spi0_Bit bs0 of Ctrl_SCK_OE and bs0_MOSI_OE is 1, bs0_MISO_The OE bit is 0. Set the P1 port direction bsck and bmosi as the output, bmiso as the input, and the chip selection pin as the output.

Data transmission process:

(1) , write spi0_Data register, write the data to FIFO and start SPI transmission automatically.

(2) , waiting for S0_Free is 1, indicating that the transmission is completed and the next byte can be sent.

Data receiving process:

(1) , write spi0_Data register, write any data to FIFO, such as 0ffh, to start a SPI transmission.

(2) , waiting for S0_Free is 1, indicating that the reception is complete, and spi0 can be read_Data gets the received data.

(3) If bs0_DATA_If dir is set to 1, the above read operation will also start the next SPI transmission, otherwise it will not be started.

14.4.2 SPI slave mode configuration

Only spi0 supports the slave mode. In the slave mode, the SCK pin is used to receive the serial clock of the connected SPI master.

(1) , set spi0, set register spi0_Bit bs0 of setup_MODE_SLV is 1 and configured as slave mode.

(2) Set spi0 control register spi0_Bit bs0 of Ctrl_SCK_OE and bs0_MOSI_OE is 0, set bs0_MISO_OE is

1Set the P1 port direction bsck, bmosi and bmiso as well as the chip selection pin as the input.When SCS chip selection is effective (low level), miso will automatically enable output.At the same time, it is recommended to set miso pin to high impedance input mode (P1_MOD_OC[6]=0、
P1_DIR_Pu [6] = 0), so miso will not output during the invalid period of chip selection, which is convenient to share SPI bus.

(3) Optional, set SPI slave mode preset data memory spi0_S_Pre, used to automatically load into the buffer for the first time after being selected for external output.After 8 serial clocks, i.e. the first data byte is transferred and exchanged, ch552 gets the first byte data (possibly command code) sent by the external SPI host, and the external SPI host exchanges to get spi0_S_Preset data (possibly state value) in pre.Register spi0_S_Bit 7 of pre will be automatically loaded into miso pin during the low level of SCK after SPI chip selection is valid. For SPI mode 0, if SPI 0 is preset by ch552_S_Bit 7 of pre, then the external SPI host can get spi0 by querying miso pin when the SPI chip is valid but data has not been transmitted_S_The preset value of bit 7 of pre, so that spi0 can be obtained by only valid SPI selection_S_The value of bit 7 of pre.

Data transmission process:

Query S0_IF_Byte or wait for interrupt, write spi0 after each SPI data byte transmission is completed_Data register, to
FIFO writes the data to be sent.Or wait for S0_Free changes from 0 to 1 to continue sending the next byte.

Data receiving process:

Query S0_IF_Byte or wait for interrupt, read spi0 after each SPI data byte transmission is completed_Data register, from
FIFO gets the received data.Query S0_R_FIFO can know whether there are any remaining bytes in FIFO.

15 ADC and voltage comparator (not applicable to ch551)

15.1 introduction to ADC

Ch552 chip provides 8-bit analog-to-digital converter, including voltage comparator and ADC module.The converter has four analog signal input channels, which can collect time-sharing data and support the range of 0 to VCC analog input voltage.

15.2 ADC register

Table 15.2.1 ADC related register list

name	address	describe	reset value
ADC_CTRL	80h	ADC control register	X0h
ADC_CFG	9AH	ADC configuration register	00h
ADC_DATA	9Fh	ADC data register	Xxh

ADC control register (ADC_CTRL)：

position	name	visit	describe	reset value
7	CMPO	RO	The result output bit of voltage comparator. If this bit is 0, the voltage of positive phase input is lower than that of opposite phase input; if this bit is 1, the voltage of positive phase input is higher than that of opposite phase input	X
6	CMP_IF	RW	The result change flag of voltage comparator. If the bit is 1, it means that the result of voltage comparator has changed, and the direct bit access is cleared	0
5	ADC_IF	RW	ADC conversion completion interrupt flag. If the bit is 1, the ADC conversion is completed and the direct bit access is cleared	0
4	ADC_START	RW	ADC start control bit, set 1 to start ADC conversion Automatic reset after ADC conversion	0
3	CMP_CHAN	RW	Voltage comparator invert input selection: 0-ain1; 1-ain3	0
2	retain	R0	retain	0
1	ADC_CHAN1	RW	High bit selection of voltage comparator normal phase input and ADC input channel	0
0	ADC_CHAN0	RW	Voltage comparator positive phase input and ADC input channel select low bit	0

Table 15.2.1 CMP normal phase input and ADC input channel table of voltage comparator

ADC_CHAN 1	ADC_CHAN 0	Select voltage comparator normal phase input and ADC input channel
0	0	AIN0 (P1.1)
0	1	AIN1 (P1.4)
1	0	AIN2 (P1.5)
1	1	AIN3 (P3.2)

ADC configuration register (ADC_CFG):

position	name	visit	describe	reset value
[7:4]	retain	R0	retain	0000b
3	ADC_EN	RW	The power control bit of ADC module. If the bit is 0, it means that the power of ADC module is turned off and enters sleep state; if the bit is 1, it means on	0
2	CMP_EN	RW	The power control bit of the voltage comparator. If the bit is 0, it means that	0

			the power supply of the voltage comparator is turned off and enters the sleep state; if the bit is 1, it means that it is on	
1	retain	R0	retain	0
0	ADC_CLK	RW	The clock frequency of the FOSC ADC is 96 bits, and the clock frequency of the FOSC ADC needs to be selected	0

ADC data register (ADC_DATA):

position	name	visit	describe	reset value
[7:0]	ADC_DATA	RO	ADC sampling result data	Xxh

15.3 ADC function

ADC sampling mode configuration steps:

(1) Setting ADC_ADC in CFG register_When en bit is 1, turn on ADC module and set BADC_CLK selects the frequency.

(2) Setting ADC_ADC in Ctrl register_Chan1 / 0, select input channel.

(3) , optional, clear interrupt flag ADC_IF。Optional, if you use interrupt mode, you also need to enable interrupt here.

(4) Setting ADC_ADC in Ctrl register_Start to start an ADC conversion.

(5) , waiting for ADC_Start becomes 0, or ADC_If is set to 1 (if it has been cleared before), it indicates that the ADC conversion is finished, and the

ADC_Data reads the result data.The data is 255 equal parts of the input voltage relative to the VCC supply voltage. For example, the resulting data is 47, indicating that the input voltage is close to 47 / 255 of the VCC voltage.If the VCC power supply voltage is uncertain, then another determined reference voltage value can be measured, and then the measured input voltage value and VCC power supply voltage value can be calculated in proportion.

(6) If the ADC is set again_Start can start the next ADC conversion.

Voltage comparator mode configuration steps:

(1) Setting ADC_CMP in CFG register_When the en bit is 1, turn on the voltage comparator module.

(2) Setting ADC_ADC in Ctrl register_Chan1 / 0 and CMP_Chan, select positive and negative input.

(3) , optional, reset flag CMP_IF。

(4) The status of CMPO bit can be queried at any time to obtain the result of the current comparator.

(5) If CMP_If becomes 1, indicating that the result of the comparator has changed.

The GPIO pin of the selected analog signal input channel must be set to high resistance input mode or open drain output mode and be in output 1 state (equivalent to high resistance input), PN_DIR_Pu [x] = 0, and it is recommended to turn off the pull-up resistor and pull-down resistor.

16 USB controller

16.1 introduction to USB controller

Ch552 is embedded with USB controller and USB transceiver, with the following features:

(1) Support USB device function, support USB 2.0 full speed 12mbps or low speed 1.5mbps;
(2) Support USB control transmission, batch transmission, interrupt transmission, synchronous / real-time transmission;
(3) Support 64 byte packets, built-in FIFO, support interrupt and DMA.

The USB related register of ch552 is divided into two parts: USB global register and USB endpoint register.

16.2 Global register

Table 16.2.1 list of USB global registers (Standard grey Subject to bouc_RESET_Sie reset control)

name	address	describe	reset value
USB_C_CTRL	91h	USB type-C configuration channel control register	0000 0000b
USB_INT_FG	D8h	USB interrupt flag register	0010 0000b
USB_INT_ST	D9h	USB interrupt status register (read only)	00xx xxxxb
USB_MIS_ST	DAh	USB miscellaneous status register (read only)	xx10 1000b
USB_RX_LEN	DBh	USB receive length register (read only)	0xxx xxxxb
USB_INT_EN	E1h	USB interrupt enable register	0000 0000b
USB_CTRL	E2h	USB control register	0000 0110b
USB_DEV_AD	E3h	USB device address register	0000 0000b

USB type-C configuration channel control register (USB_C_CTRL): (ch551 not applicable)

position	name	visit	describe	reset value
7	bVBUS2_PD_EN	RW	This bit is 1 to enable the internal 10K pull-down resistance of vbus2 pin; it is 0 disable	0
6	bUCC2_PD_EN	RW	This bit is 1 to enable the internal 5.1k pull-down resistance of ucc2 pin; it is 0 disable	0
5	bUCC2_PU1_EN	RW	This bit is the internal pull-up resistance control selection high bit of ucc2 pin	0
4	bUCC2_PU0_EN	RW	This bit is the low bit selected by the internal pull-up resistance control of the ucc2 pin	0
3	bVBUS1_PD_EN	RW	This bit is 1 to enable the internal 10K pull-down resistance of vbus1 pin; it is 0 disable	0
2	bUCC1_PD_EN	RW	This bit is 1 to enable the internal 5.1k pull-down resistance of UCC1 pin; it is 0 disable	0

1	bUCC1_PU1_EN	RW	This bit is the internal pull-up resistance control selection high bit of UCC1 pin	0
0	bUCC1_PU0_EN	RW	This bit is the low bit selected by the internal pull-up resistance control of UCC1 pin	0

By buccn_PU1_EN and buccn_PU0_EN selects the pull-up resistance inside the uccn pin.

bUCCn_PU1_EN	bUCCn_PU0_EN	Select the pull-up resistance inside the uccn pin
0	0	Internal pull-up resistance is prohibited
0	1	Enable internal 56K Ω pull-up resistor, indicating the default USB current
1	0	Enable internal 22K Ω pull-up resistance, indicating that 1.5A current can be provided
1	1	Enable internal 10K Ω pull-up resistance, indicating that 3A current can be provided

The above USB type-C pull-up and pull-down resistors are independent of PN_DIR_When a pin is used for USB type-C, the port pull-up resistance corresponding to the pin should be prohibited. It is recommended to enable the high resistance input mode for the pin (to avoid low or high-level output of the pin).

For detailed control and input detection of USB type-C configuration channel, please refer to USB type-C application instructions and routines.

USB interrupt flag register (USB_INT_FG):

position	name	visit	describe	reset value
7	U_IS_NAK	RO	If this bit is 1, it means that NAK busy response is received during current USB transmission; if this bit is 0, it means non NAK response is received	0
6	U_TOG_OK	RO	The current USB transmission Data0 / 1 synchronization flag matching status. If the bit is 1, the data is valid; if the bit is 0, it means that the data is not synchronized, and the data may be invalid	0
5	U_SIE_FREE	RO	The idle state bit of USB protocol processor. If the bit is 0, it means busy and in progress USB transmission; if this bit is 1, it means USB is idle	1
4	UIF_FIFO_OV	RW	USB FIFO overflow interrupt flag bit, the bit 1 indicates FIFO overflow interrupt; the bit is 0 Non interrupt.Clear direct bit access or write 1	0
3	retain	RO	retain	0
2	UIF_SUSPEND	RW	USB bus hang or wake-up event interrupt flag bit, this bit is 1 to indicate there is an interrupt, the interrupt is triggered by USB hang event or wake-up event; if this bit is 0, it means no interrupt.Clear direct bit access or write 1	0
1	UIF_TRANSFE	RW	USB transmission completion interrupt flag bit,	0

	R		this bit is 1 to indicate there is an interrupt, the interrupt is triggered by a USB transmission completion; the bit 0 means no interruption.Clear direct bit access or write 1	
0	UIF_BUS_RST	RW	USB bus reset event interrupt flag bit, this bit is 1 indicates there is an interrupt, the interrupt is triggered by USB bus reset event; the bit 0 means no interrupt.Clear direct bit access or write 1	0

USB interrupt status register (USB_INT_ST)：

position	name	visit	describe	reset value
7	bUIS_IS_NAK	RO	If this bit is 1, it indicates that NAK busy response is received during current USB transmission. Same as U_IS_NAK	0
6	bUIS_TOG_OK	RO	The current USB transmission Data0 / 1 synchronization flag matching status. If this bit is 1, it means synchronization; if this bit is 0, it means that it is not synchronized.Same as U_TOG_OK	0
5	bUIS_TOKEN1	RO	Token PID ID high bit of current USB transfer transaction	X
4	bUIS_TOKEN0	R0	Token PID identification low bit of current USB transfer transaction	X
[3:0]	MASK_UIS_ENDP	RO	The number of the current USB transaction is 0; 1111Represents endpoint 15	xxxxb

bUIS_Taken1 and bouis_Token 0 makes up mask_UIS_Token: the token used to identify the current USB transfer transaction. PID: 00 indicates out packet; 01 represents sof package; 10 represents in package; 11 represents setup package.

USB miscellaneous status register (USB_MIS_ST)：

position	name	visit	describe	reset value
[7:6]	retain	RO	retain	Xxb
5	bUMS_SIE_FREE	RO	The idle state bit of USB protocol processor. If the bit is 0, it means busy, positive USB transmission is in progress; if this bit is 1, it means USB is idle.with U_SIE_FREE	1
4	bUMS_R_FIFO_RDY	RO	USB receive FIFO data ready status bit, this bit is 0 to receive FIFO is empty; a bit of 1 indicates that the received FIFO is not empty	0
3	bUMS_BUS_RESET	RO	USB bus reset status bit: 0 indicates that there is no USB bus reset; 1 indicates that	1

			USB bus is currently being reset	
2	bUMS_SUSPEND	RO	USB suspend status bit. If the bit is 0, it means there is current USB activity Bit 1 indicates that there has been no USB activity for some time and the request is pending	0
[1:0]	retain	RO	retain	00B

USB receive length register (USB_RX_LEN):

position	name	visit	describe	reset value
[7:0]	bUSB_RX_LEN	RO	The number of bytes of data received by the current USB endpoint	Xxh

USB interrupt enable register (USB_INT_EN):

position	name	visit	describe	reset value
7	bUIE_DEV_SOF	RW	This bit is 1 to enable to receive sof packet interrupts; 0 to disable	0
6	bUIE_DEV_NAK	RW	This bit is 1 to enable NAK interrupt to be received; 0 to disable	0
5	retain	RO	retain	0
4	bUIE_FIFO_OV	RW	This bit is 1 enable FIFO overflow interrupt; this bit is 0 off enable	0
3	retain	RO	retain	0
2	bUIE_SUSPEND	RW	This bit is 1 to enable USB bus suspend or wake-up event interrupt; 0 to disable	0
1	bUIE_TRANSFER	RW	This bit is 1 to enable USB transmission to complete interrupt; this bit is 0 to disable	0
0	bUIE_BUS_RST	RW	This bit is 1 to enable USB bus reset event interrupt; this bit is 0 disable	0

USB control register (USB_CTRL):

position	name	visit	describe	reset value
7	retain	RO	retain	0
6	bUC_LOW_SPEED	RW	USB bus signal transmission rate selection bit: 0 selects full speed 12mbps; 1 selects low speed 1.5mbps	0
5	bUC_DEV_PU_EN	RW	USB device enable and internal pull-up resistor control bit. If this bit is 1, USB device transmission is enabled and internal pull-up resistor is enabled	0
5	bUC_SYS_CTRL1	RW	USB system control high position	0
4	bUC_SYS_CTRL0	RW	USB system control low position	0

3	bUC_INT_BUSY	RW	USB transmission completion interrupt flag is not cleared before the auto pause enable bit 1In the interrupt flag UIF_If transfer is not cleared, it will automatically pause and answer busy NAK automatically; if this bit is 0, it will not pause	0
2	bUC_RESET_SIE	RW	USB protocol processor software reset control bit, if this bit is 1, the USB protocol processor and most USB control registers are forced to be reset, and software reset is required	1
1	bUC_CLR_ALL	RW	This bit is 1 to clear the USB interrupt flag and FIFO, which needs to be cleared by software	1
0	bUC_DMA_EN	RW	This bit enables DMA and DMA interrupt of USB, and turns off enable for 0	0

By BUC_SYS_Ctrl1 and bouc_SYS_Ctrl0 forms the USB system control combination

bUC_SYS_CTRL1	bUC_SYS_CTRL0	USB system control description
0	0	Disable USB device function and turn off internal pull-up resistor
0	1	Enable USB device function, turn off internal pull-up, need to add external pull-up
1	X	Enable USB device function and enable internal 1.5k Ω pull-up resistor.The pull-up resistor takes precedence over the pull-down resistor and can also be used in GPIO mode

USB device address register (USB_DEV_AD)：

position	name	visit	describe	reset value
7	bUDA_GP_BIT	RW	USB universal flag bit: user can customize, can be reset or set by software	0
[6:0]	MASK_USB_ADDR	RW	The address of the USB device	00h

16.3 Endpoint register

Ch552 provides five groups of bidirectional endpoints: 0, 1, 2, 3, and 4. The maximum packet length of all endpoints is 64 bytes.

Endpoint 0 is the default endpoint. It supports controlling transmission. Sending and receiving share a 64 byte data buffer.

Endpoint 1, endpoint 2 and endpoint 3 each contain a sending endpoint in and a receiving endpoint out. The sending and receiving have an independent 64 byte or double 64 byte data buffer, which supports control transmission, batch transmission, interrupt transmission and real-time / synchronous transmission.

Endpoint 4 includes a sending endpoint in and a receiving endpoint out. Each sending and receiving has an independent 64 byte data buffer, which supports control transmission, batch transmission, interrupt transmission and real-time / synchronous transmission.

Each endpoint has a control register uepn_CTRL and transmit length register uepn_T_Len (n = 0 / 1 / 2 / 3 / 4) is used to set the synchronization trigger bit, response to out transaction and in transaction, and the length of sent data.

As a necessary USB device, the pull-up resistor of USB bus can be set by software at any time, when the USB control register USB_BUC in Ctrl_DEV_PU_When en is set to 1, ch552 is in accordance with boud_LOW_Speed is the DP pin of USB bus or
The DM pin connects the pull-up resistor and enables the USB device function.

When USB reset, USB hang or wake-up events are detected, or when USB successfully processes data transmission or data reception, the USB protocol processor will set the corresponding interrupt flag and generate interrupt request.Application program can query and analyze interrupt flag register USB directly or in USB interrupt service program_INT_FG, according to UIF_BUS_RST and UIF_Suspend is processed accordingly; and if UIF_If transfer is valid, you need to continue analyzing USB interrupt status register USB_INT_St, according to the current endpoint number mask_UIS_Endp and current transaction token PID identify mask_UIS_Token is processed accordingly.If the synchronization trigger bit BUEP of the out transaction of each endpoint is set in advance_R_Tog, then you can go through U_TOG_Uibok or_TOG_OK determines whether the synchronization trigger bit of the currently received packet matches the synchronization trigger bit of the endpoint. If the data is synchronized, the data is valid; if the data is not synchronized, the data should be discarded.After processing the USB sending or receiving interrupt, the synchronization trigger bit of the corresponding endpoint should be correctly modified to synchronize the next sent packets and detect whether the next received packets are synchronized. In addition, by setting the BUEP_AUTO_Tog can automatically flip the corresponding synchronous trigger bit after successful sending or receiving.

The data to be sent by each endpoint is in its own buffer, and the data length to be sent is set independently in uepn_T_In len, the data received by each endpoint is in its own buffer, but the data length received is in the USB receive length register USB_RX_In len, it can be distinguished according to the current endpoint number when USB receives interrupt.

Table 16.3.1 USB device endpoint related registers list (Standard grey Subject to bouc_RESET_Sie reset control)

name	address	describe	reset value
UDEV_CTRL	D1h	USB device physical port control register	10xx 0000b
UEP1_CTRL	D2h	Endpoint 1 control register	0000 0000b
UEP1_T_LEN	D3h	Endpoint 1 transmit length register	0xxx xxxxb
UEP2_CTRL	D4h	Endpoint 2 control register	0000 0000b
UEP2_T_LEN	D5h	End point send register length 2	0000 0000b
UEP3_CTRL	D6h	Endpoint 3 control register	0000 0000b
UEP3_T_LEN	D7h	Endpoint 3 transmit length register	0xxx xxxxb
UEP0_CTRL	DCh	Endpoint 0 control register	0000 0000b
UEP0_T_LEN	DDh	Endpoint 0 send length register	0xxx xxxxb
UEP4_CTRL	DEh	Endpoint 4 control register	0000 0000b
UEP4_T_LEN	DFh	Endpoint 4 transmit length register	0xxx xxxxb
UEP4_1_MOD	EAh	Endpoint 1,4 mode control register	0000 0000b
UEP2_3_MOD	EBh	Endpoint 2,3 mode control register	0000 0000b
UEP0_DMA_H	EDh	Endpoint 0 and 4 buffer start address high byte	0000 00xxb

UEP0_DMA_L	ECh	Endpoint 0 and 4 buffer start address low byte	xxxx xxxxb
UEP0_DMA	ECh	UEP0_DMA_L and uep0_DMA_H constitutes a 16 bit SFR	0xxxh
UEP1_DMA_H	EFh	Endpoint 1 buffer start address high byte	0000 00xxb
UEP1_DMA_L	EEh	Endpoint 1 buffer start address low byte	xxxx xxxxb
UEP1_DMA	EEh	UEP1_DMA_L and uep1_DMA_H constitutes a 16 bit SFR	0xxxh
UEP2_DMA_H	E5h	Endpoint 2 buffer start address high byte	0000 00xxb
UEP2_DMA_L	E4h	Endpoint 2 buffer start address low byte	xxxx xxxxb
UEP2_DMA	E4h	UEP2_DMA_L and uep2_DMA_H constitutes a 16 bit SFR	0xxxh
UEP3_DMA_H	E7h	Endpoint 3 buffer start address high byte	0000 00xxb
UEP3_DMA_L	E6h	Endpoint 3 buffer start address low byte	xxxx xxxxb
UEP3_DMA	E6h	UEP3_DMA_L and uep3_DMA_H constitutes a 16 bit SFR	0xxxh

USB device physical port control register (udev_CTRL) is affected by BUC_RESET_Sie reset control:

position	name	visit	describe	reset value
7	bUD_PD_DIS	RW	USB device port UDP / UDM pin internal pull-down resistance disable bit, this bit is 1 disable internal pull-down resistance; this bit is 0 enable internal pull-down resistance.This bit is not subject to busb_IO_Can also be used for pull-down, GPIO control mode	1
6	retain	RO	retain	0
5	bUD_DP_PIN	RO	Current UDP pin status, 0 indicates low level; 1 indicates high level	X
4	bUD_DM_PIN	RO	Current UDM pin status: 0 indicates low level; 1 indicates high level	X
3	retain	RO	retain	0
2	bUD_LOW_SPEED	RW	USB device physical port low speed mode enable bit, this bit is 1 to select 1.5mbps low speed mode; this bit is 0 to select 12mbps full speed mode	0
1	bUD_GP_BIT	RW	General mark bit of equipment: user can define it by himself, and can be reset or set by software	0
0	bUD_PORT_EN	RW	USB device physical port enable bit, this bit is 1 enable physical port; this bit is 0Disable physical port	0

Endpoint n control register (uepn_CTRL)：

position	name	visit	describe	reset value
7	bUEP_R_TOG	RW	The expected synchronous trigger bit of	0

			receiver (processing setup / out transaction) of USB endpoint n, where 0 indicates the expected Data0; 1 indicates the expected data1	
6	bUEP_T_TOG	RW	The synchronous trigger bit prepared by the transmitter (processing in transaction) of USB endpoint n. if the bit is 0, Data0 is sent; if 1 is 1, data1 is sent	0
5	retain	RO	retain	0
4	bUEP_AUTO_TOG	RW	The synchronization trigger bit can be automatically flipped to enable control bit. If the bit is 1, it means that the corresponding synchronous trigger bit will be automatically flipped after successful transmission or reception; if it is 0, it will not be automatically flipped, but can be manually switched.Only supports endpoint 1 / 2 / 3	0
3	bUEP_R_RES1	RW	Response control bit of receiver of endpoint n to setup / out transaction	0
2	bUEP_R_RES0	RW	The receiver of endpoint n controls the low bit of response to setup / out transaction	0
1	bUEP_T_RES1	RW	Response control bit of sender of endpoint n to in transaction	0
0	bUEP_T_RES0	RW	The response control bit of the sender of endpoint n to in transaction	0

By BUEP_R_Res1 and BUEP_R_Mask composed of res0_UEP_R_Res is used to control the response mode of receiver of endpoint n to setup / out transaction: 00 indicates ACK or ready; 01 indicates timeout / no response, which is used to realize real-time / synchronous transmission of non endpoint 0; 10 indicates ACK or busy response; 11 indicates reply stand or error.

By BUEP_T_Res1 and BUEP_T_Mask composed of res0_UEP_T_Res is used to control the response mode of the transmitter of endpoint n to in transaction: 00 means to reply Data0 / data1 or data ready and expect ack; 01 means to reply Data0 / data1 and expect no response, which is used to realize real-time / synchronous transmission of non endpoint 0; 10 means to reply NAK or busy; 11 to reply to stand or error.

Endpoint N transmit length register (uepn_T_LEN)：

position	name	visit	describe	reset value
[7:0]	bUEPn_T_LEN	RW	Set the number of data bytes to be sent by USB endpoint n (n = 0 / 1 / 3 / 4)	Xxh
	bUEP2_T_LEN		Set the number of data bytes that USB endpoint 2 is ready to send	00h

USB endpoint 1,4 mode control register (uep4_1_MOD)：

position	name	visit	describe	reset value
7	bUEP1_RX_EN	RW	If the bit is 0, the end point 1 is prohibited from receiving; if it is 1, the end point 1	0

			receiving (out) is enabled	
6	bUEP1_TX_EN	RW	If the bit is 0, the end point 1 is forbidden to send; if the bit is 1, enable the end point 1 to send (in)	0
5	retain	RO	retain	0
4	bUEP1_BUF_MOD	RW	Endpoint 1 data buffer mode control bit	0
3	bUEP4_RX_EN	R0	If this bit is 0, it prevents endpoint 4 from receiving; if it is 1, it enables endpoint 4 to receive (out)	0
2	bUEP4_TX_EN	RW	If this bit is 0, it will prevent endpoint 4 from sending; if it is 1, enable endpoint 4 to send (in)	0
[1:0]	retain	RO	retain	00B

By buep4_RX_EN and buep4_TX_The en combination controls the data buffer mode of USB endpoints 0 and 4. Refer to the table below.

Table 16.3.2 endpoint 0 and 4 buffer patterns

bUEP4_RX_EN	bUEP4_TX_EN	Structure description: UEP 0_DMA is arranged from low to high
0	0	Endpoint 0 single 64 byte transmit receive common buffer (in and out)
1	0	Endpoint 0 single 64 byte receive buffer; endpoint 4 single 64 byte receive buffer (out)
0	1	Endpoint 0 single 64 byte transmit and receive shared buffer; endpoint 4 single 64 byte transmit buffer (in)
1	1	Endpoint 0 single 64 byte receive buffer (out); endpoint 4 single 64 byte receive buffer (out); endpoint 4 single 64 byte transmit buffer (in).All 192 bytes are arranged as follows: UEP0_DMA + 0 address: end point 0 is used for receiving and sending; UEP0_DMA + 64 address: received by endpoint 4; UEP0_DMA + 128 address: endpoint 4 transmit

USB endpoint 2,3 mode control register (uep2_3_MOD)：

position	name	visit	describe	reset value
7	bUEP3_RX_EN	RW	The 3 bit is a receive end point; the receive end point is disabled	0
6	bUEP3_TX_EN	RW	If this bit is 0, it will prevent endpoint 3 from sending; if it is 1, enable endpoint 3 to send (in)	0
5	retain	RO	retain	0
4	bUEP3_BUF_MOD	RW	Endpoint 3 data buffer mode control bit	0
3	bUEP2_RX_EN	R0	If this bit is 0, it prevents endpoint 2 from receiving; if it is 1, enable endpoint 2 to receive (out)	0
2	bUEP2_TX_EN	RW	If the bit is 0, the sending of endpoint 2 is	0

			prohibited; if it is 1, the sending of endpoint 2 is enabled (in)	
1	retain	RO	retain	0
0	bUEP2_BUF_MOD	RW	Endpoint 2 data buffer mode control bit	0

By buepn_RX_EN and buepn_TX_EN and buepn_BUF_Mod (n = 1 / 2 / 3) combination respectively controls the data buffer mode of USB endpoint 1, 2 and 3. Refer to the table below.Among them, double 64 byte buffer mode, USB data transmission will be based on the BUEP_* *Tog = 0 selects the first 64 byte buffer according to BUEP_* *Tog = 1, select the last 64 byte buffer to realize automatic switching.Table 16.3.3 endpoint n buffer mode (n = 1 / 2 / 3)

bUEPn_RX_EN	bUEPn_TX_EN	bUEPn_BUF_MOD	Structure description: uepn_DMA is arranged from low to high
0	0	X	The endpoint is disabled and uepn is not used_DMA buffer
1	0	0	Receive buffer (64 bytes)
1	0	1	Double 64 byte receive buffer, through BUEP_R_Tog selection
0	1	0	Single 64 byte send buffer (in)
0	1	1	Double 64 byte send buffer, through BUEP_T_Tog selection
1	1	0	Single 64 byte receive buffer; single 64 byte transmit buffer
1	1	1	Double 64 byte receive buffer, through BUEP_R_Tog selection; double 64 byte send buffer, through BUEP_T_Tog selection. All 256 bytes are arranged as follows: UEPn_DMA + 0 address: BUEP_R_When tog = 0, the endpoint receives; UEPn_DMA + 64 address: BUEP_R_When tog = 1, the endpoint receives; UEPn_+ BEP address: 128_T_When tog = 0, the endpoint sends; UEPn_DMA + 192 address: BUEP_T_When tog = 1, the endpoint sends

USB endpoint n buffer start address (uepn_DMA)(n=0/1/2/3)：

position	name	visit	describe	reset value
[7:0]	UEPn_DMA_H	RW	The starting address of endpoint n buffer is high byte, only the lower 2 bits are valid, and the high 6 bits are fixed to 0	0xh
[7:0]	UEPn_DMA_L	RW	Endpoint n buffer start address low byte	Xxh

Note: the length of buffer for receiving data > = min (the maximum packet length that may be received + 2 bytes, 64 bytes)

17 Touch the key

17.1 introduction to touch key

Ch552 chip provides capacitance detection module and related timer, with 6 input channels, and supports capacitance range of 5pf ～ 150pF。The self capacitance mode can support up to 6 touch buttons, and the mutual capacitance mode can support up to 15 touch buttons.

17.2 touch key register

Table 17.2.1 list of touch key related registers

name	address	describe	reset value
TKEY_CTRL	C3h	Touch key control register	X0h
TKEY_DATH	C5h	Touch key data high byte (read only)	00h
TKEY_DATL	C4h	Touch key data low byte (read only)	Xxh
TKEY_DAT	C4h	TKEY_Datl and tkey_Dath forms a 16 bit SFR	00xxh

Touch key control register (tkey_CTRL)：

position	name	visit	describe	reset value
7	bTKC_IF	RO	Timing interrupt flag.If btkd_If CHG = 0, it will automatically set 1 to request interrupt at the end of the current timing cycle. When the preparation phase is finished, it will be reset automatically, or by writing tkey_CTRL clear.If btkd_If CHG = 1, it will clear automatically, do not request interrupt, skip the current cycle, and then re prepare and detect in the next cycle, and automatically set 1 to request interrupt at the end of the next cycle	X
[6:5]	retain	RO	retain	00B
4	bTKC_2MS	RW	Cycle selection of capacitance detection timer: 0-1ms; 1-2ms. The first 87us of each cycle is the preparation stage and the remaining time detection stage. The above time is based on FOSC = 24MHz	0
3	retain	RO	retain	0
2	bTKC_CHAN2	RW	Touch the button to select the high position of capacitance detection input	0
1	bTKC_CHAN1	RW	Touch the button to select the middle position of capacitance detection input	0
0	bTKC_CHAN0	RW	Touch the button to select the low position of capacitance detection input	0

By btkc_CHAN2～bTKC_Chan0 selects the input channel of capacitance detection by touching the button.

bTKC_CHAN2	bTKC_CHAN1	bTKC_CHAN0	Select the input channel for capacitance detection of touch button
0	0	0	Turn off the power supply of the capacitance detection module and only use it as an independent timing interrupt with a period of 1ms or 2ms
0	0	1	TIN0（P1.0）
0	1	0	TIN1（P1.1）
0	1	1	TIN2（P1.4）
1	0	0	TIN3（P1.5）
1	0	1	TIN4（P1.6）
1	1	0	TIN5（P1.7）
1	1	1	Turn on the power supply of capacitance detection module, but do not connect any channel

Touch key data register (tkey_DAT)：

position	name	visit	describe	reset value
7	bTKD_CHG TKEY_DATH[7]	RO	Touch key controls the change flag.This bit of 1 indicates tkey_The CTRL is rewritten in the capacitance detection phase, which may lead to tkey_Dat data is invalid and btkc will not be set at the end of the current cycle_IF。This bit is automatically cleared at the end of the preparation phase of each timing cycle, and this bit needs to be masked when data is fetched	0
6	retain	RO	retain	0
[5:0]	TKEY_DATH	RO	Touch key data high byte.At the end of the preparation stage of each timing cycle, it is automatically cleared; in the capacitance detection phase, it is automatically counted; in the preparation stage, the data is kept unchanged, so that the timing interrupt program can read	00h
[7:0]	TKEY_DATL	RO	Touch key data low byte.At the end of the preparation stage of each timing cycle, it is automatically cleared; in the capacitance detection phase, it is automatically counted; in the preparation stage, the data is kept unchanged, so that the timing interrupt program can read	Xxh

17.3 touch key function

capacitance detection steps:

(1) Setting tkey_Btkc in the CTRL register_2ms and btkc_CHAN2～bTKC_Chan0, select period and input channel.The GPIO pin of the selected input channel must be set to high resistance input mode or open drain output mode and be in output 1 state (equivalent to high resistance input), PN_DIR_PU[x]=0。

(2) , clear btkc_If and enable interrupt ie_Tkey waits for timing interrupt or queries btkc actively_If enters interrupt program.

(3) The btkc will be set automatically after the capacitance detection of the current channel is completed_If request interrupt, and enter the next cycle preparation phase, and keep tkey_The dat data remains unchanged about 87us.

(4) , enter the interrupt program, first from tkey_Dat reads the capacitance data of the current channel and shields the highest bit btkd_CHG, the data is a relative value, which is inversely proportional to the capacitance. When the touch button is pressed, the data is smaller than that when the button is not pressed.

(5) Setting tkey_Btkc in the CTRL register_2ms and btkc_CHAN2～bTKC_Chan 0, select the next input channel.This clear operation will automatically write to TKBC_If, end interrupt request.

(6) Tkey read with step (4)_Dat data is compared with the data saved before when there is no key in the channel to judge whether the capacitance changes and whether there is a key pressed.

(7) Interrupt return. After the capacitance detection of the next channel is completed, turn to step (3).

18, parameters

18.1 Absolute maximum (critical value or exceeding absolute maximum value may lead to abnormal operation or even damage of the chip)

name	Parameter description	minimum value	Maximum	Company
TA	Ambient temperature at work	-40	85	Temperature
TS	Ambient temperature during storage	-55	125	Temperature
VCC	Power supply voltage (VCC to power, GND to ground)	-0.4	5.8	V
VIO	Voltage on input or output pins other than P3.6 / P3.7	-0.4	VCC+0.4	V
VIOU	Voltage on P3.6 / P3.7 input or output pins	-0.4	V33+0.4	V

18.2 Electrical parameters 5V (test conditions: TA = 25 ℃, VCC = 5V, Fsys = 6mhz)

name	Parameter description		minimum value	Typical value	Maximum	Company
VCC5	VCC pin supply voltage	V33 external capacitance only	3.7	5	5.5	V
V33	Internal USB power regulator output voltage		3.14	3.27	3.4	V

ICC24M5	Fsys = total power supply current at 24MHz	8	11		MA
ICC6M5	Fsys = total power supply current at 6mhz	4	6		MA
ICC750K5	Fsys = total power supply current at 750khz	2	3		MA
ISLP5	Total power supply current after sleep		0.1	0.2	MA
ISLP5L	VCC = V33 = 5V, and external crystal clock, and bldo3v3_Off = 1 turn off LDO, total power supply current after complete sleep		0.008	0.02	MA
IADC5	Working current of ADC module		200	800	UA
ICMP5	Working current of voltage comparator module		100	500	UA
ITKEY5	Touch the button to detect the working current of capacitance detection module		150	250	UA
VIL5	Low level input voltage	-0.4		1.2	V
VIH5	High level input voltage	2.4		VCC+0.4	V
VOL5	Low level output voltage (12mA suction current)			0.4	V
VOH5	8 mA output voltage	VCC-0.4			V
VOH5U	P3.6 / P3.7 high level output voltage (8Ma output current)	V33-0.4			V
IIN	Input current without pull-up input	-5	0	5	UA
IDN5	Input current with pull down resistor input	-35	-70	-140	UA
IUP5	Input current with pull-up resistor input	35	70	140	UA
IUP5X	Input current when the pull-up input is flipped from low to high	250	400	600	UA
Vpot	Threshold voltage of power on reset	2.1	2.3	2.5	V

18.3 Electrical parameters 3.3V (test conditions: TA = 25 ℃, VCC = V33 = 3.3V, Fsys = 6mhz)

name	Parameter description		minimum value	Typical value	Maximum	Company
VCC3	VCC pin supply voltage	V33 short circuit to VCC, turn on USB	3.0	3.3	3.6	V
		V33 short circuit to VCC, turn off USB	2.7	3.3	3.6	V
ICC16M3	Fsys = total power supply current at 16mhz		4	6		MA
ICC6M3	Fsys = total power supply current at 6mhz		2	4		MA

ICC750K3	Fsys = total power supply current at 750khz	1	2		MA
ISLP3	Total power supply current after sleep		0.07	0.15	MA
ISLP3L	bLDO3V3_Off = 1 turn off LDO, total power supply current after complete sleep		0.004	0.01	MA
IADC3	Working current of ADC module		150	500	UA
ICMP3	Working current of voltage comparator module		70	300	UA
ITKEY3	Touch the button to detect the working current of capacitance detection module		130	200	UA
VIL3	Low level input voltage	-0.4		0.8	V
VIH3	High level input voltage	1.9		VCC+0.4	V
VOL3	Low level output voltage (8Ma suction current)			0.4	V
VOH3	High level output voltage (5mA output current)	VCC-0.4			V
VOH3U	P3.6 / P3.7 high level output voltage (8Ma output current)	V33-0.4			V
IIN	Input current without pull-up input	-5	0	5	UA
IDN3	Input current with pull down resistor input	-15	-30	-60	UA
IUP3	Input current with pull-up resistor input	15	30	60	UA
IUP3X	Input current when the pull-up input is flipped from low to high	100	170	250	UA
Vpot	Threshold voltage of power on reset	2.1	2.3	2.5	V

18.4 Timing parameters (test conditions: TA = 25 ℃, VCC = 5V or VCC = V33 = 3.3V, Fsys = 6mhz)

name	Parameter description	minimum value	Typical value	Maximum	Company
Fxt	External crystal frequency or Xi input clock frequency	6	24	25	MHz
Fosc	Calibrated internal clock frequency when V33 = 3V ~ 3.6V	23.64	24	24.36	MHz
Fosc28	Calibrated internal clock frequency when V33 = 2.8V ~ 3V	23.28	24	24.72	MHz
Fosc27	Calibrated internal clock frequency at V33 = 2.7V	21	24	25	MHz
Fpll	PLL frequency after internal frequency doubling	24	96	100	MHz
Fusb4x	When using USB device function, USB sampling clock frequency	47.04	48	48.96	MHz

Fsys	System main frequency clock frequency (VCC > = 4.4V)	0.1	6	24	MHz
	Clock frequency of system main frequency (4.4V > VCC > = 3.3V)	0.1	6	16	MHz
	System main frequency clock frequency (VCC < 3.3V)	0.1	6	12	MHz
Tpor	Power on reset delay	9	11	15	MS
Trst	Width of effective reset signal input from RST	70			NS
Trdl	Thermal reset delay	30	45	60	US
Twdc	Calculation formula of watchdog overflow period / timing period	65536 * (0x100 - WDOG_COUNT) / Fsys			
Tusp	检测 USB 自动挂起时间	4	5	6	mS
Twak	芯片睡眠后唤醒完成时间	1	2	10	uS

19、修改记录

版本	日期	说明
V1.0	2016.12.20	初版发行
V1.1	2017.09.12	最高系统主频调整为 24MHz，更新 8.2，18.4
V1.2	2017.12.16	概述中增加 CH552/CH551 区别表，修改一些表头形式
V1.3	2018.03.20	1 概述中 CH552/1 区别表形式修改，修改表 18.4， 5.3 堆栈指针(SP)修正错别字，6.2 增加 Data Flash 建议
V1.4	2018.08.28	更新 18.4 中 Fosc27