Three technologies on one chip make a broadband amplifier

Bipolar transistors, an MOS capacitor, and a thin-film resistor combine to eliminate the bugaboo of emitter-lead inductance; even the package lead inductance is utilized, as a tee-coil for interstage peaking

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☐ The latest in bipolar, thin-film and metal-oxide-semiconductor technologies complement each other to pack a gigahertz-bandwidth, direct-coupled amplifier, with electronically controllable gain and polarity, onto a single chip just 40 mils square. The circuit is mounted in a new high-dissipation package, and uses parasitic lead inductances and etched-circuit-board capacitances to provide broad bandwidth and resistive input impedance at low cost. The nominal gain of 9 decibels provides a gain-bandwidth product of 2.8 GHz.

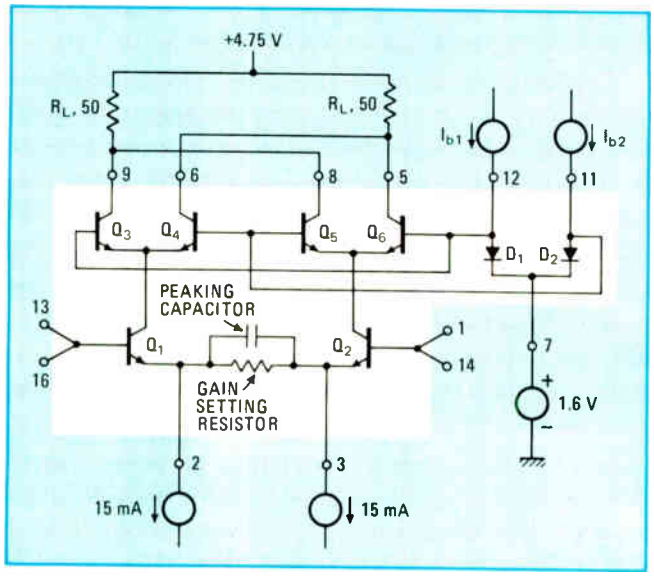
Until recently, linear bipolar integrated transistors were so much slower than their discrete counterparts that the discrete approach was always used for high-speed amplifiers. The fastest of such amplifiers still use discrete devices. This approach, however, is prohibitively expensive where a large number of stages is involved in a high-volume, highly competitive field such as commercial instrumentation.

Obviously, a fully integrated approach to broad-band multistage amplifiers would be economically the most attractive, but it has several technical drawbacks:

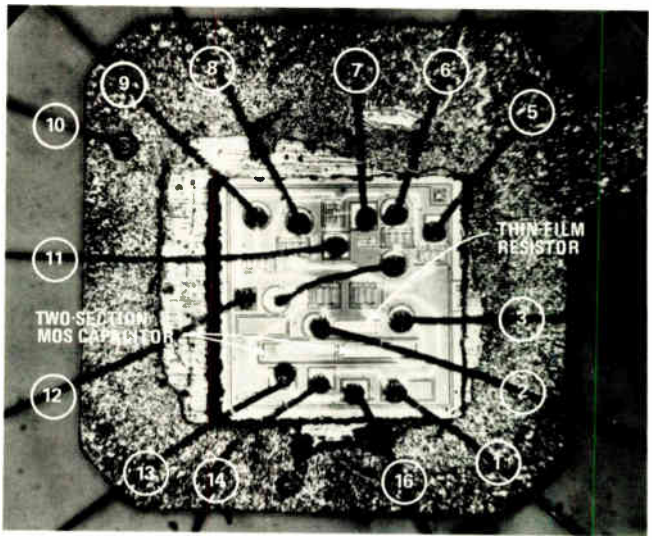
- If two or more stages are integrated onto a single chip, there is no possibility of interstage inductive peaking—which can afford a three-fold improvement in gain-bandwidth product.
- Adjustment of transient response is difficult, if not impossible.
- The package imposes an unnecessary power limitation on the circuit.
- Circuit yields will be low because of the very tight tolerances required to fabricate the fastest transistors.

If a single-integrated-stage approach is taken instead, another difficulty arises. The lead inductance entering and leaving the package limits the bandwidth unless it can also be used for needed interstage peaking. Even so, inductance in series with the emitter's gain-setting resistor and the peaking capacitor is the most serious limitation on circuit bandwidth, because of the low impedance level of the emitter circuit. If, however, both the resistor and capacitor can be integrated onto the IC chip, this limitation can be removed along with the cost of a miniature resistor and capacitor. This is the approach taken here. It has proved high in performance as well as economical.

The configuration of the circuit (Fig. 1) is that of a cascode amplifier utilizing one of the Gilbert multiplier



1. Broadband. Basic IC is a cascode amplifier in a Gilbert multiplier configuration. Because gain-setting resistor and peaking capacitor are integrated onto chip, emitter lead inductance is minimized, and bandwidth is greatly increased.



2. Three in one. Bipolar amplifier chip includes MOS capacitor and stable thin-film Nichrome resistor. Note that input signals applied to pins 1 and 13 loop through both package and circuit and come out at pins 14 and 16, respectively.

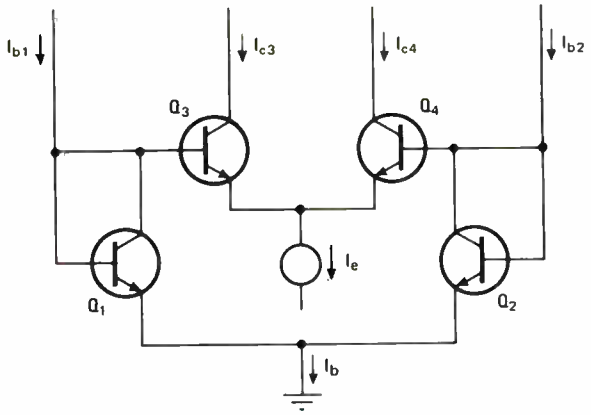
The Gilbert multiplier

The Gilbert multiplier shown here exploits the known logarithmic voltage-current characteristics of one semiconductor junction so as to linearize the current flow in another junction. Transistors Q_3 and Q_4 may be considered as being voltage-driven by current-driven transistors Q_1 and Q_2.

Starting with the equation $V_{be} = (mkT/q)\ln(I_c/I_s)$, where I_s is a characteristic of the transistor, Gilbert[1] shows, by summing the voltages around the Q_1–Q_2 loop, that $(I_{c3}/I_{b1}) = (I_{c4}/I_{b2}) = (I_e/I_b)$.

When Q_1 and Q_2 control two pairs of transistors which are themselves differentially driven, as in Fig. 1 in the accompanying text, then the over-all stage gain can be completely controlled by the two bias currents (I_{b1} and I_{b2} of Fig. 1). For example, when the two currents are equal, signals from Q_1 and Q_2 cancel in the output, and the gain is zero.

If the currents constitute a push-pull signal source applied to the control bases (pins 11 and 12 of Fig. 1) and a voltage applied between Q_1 and Q_2 is a second signal source, the output voltage between pins 5 and 9 is the product of the two signals. This circuit is the basis of most of the multipliers on the market today.

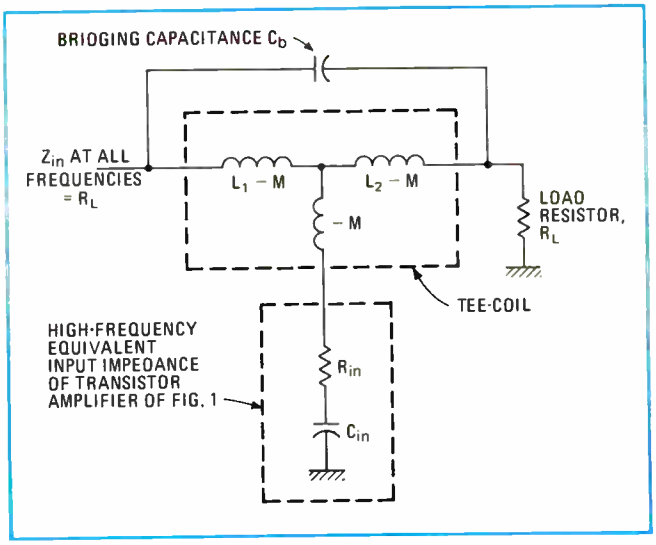


schemes.[1]. In normal operation, pin 12 (known as a control base) is connected to current source I_{b1}. I_{b2} is zero. The input is connected between pins 1 and 13, and the output is taken between pins 5 and 9. Under these conditions, transistors Q_4 and Q_5 and diode D_2 are off, and may be ignored. The resulting configuration is the standard cascode amplifier, with Q_3 and Q_6 acting as the common-base output transistors.

If I_{b1} is off and I_{b2} is on, signal current from Q_1 and Q_2 flows in Q_4 and Q_5 respectively. The configuration is still that of the cascode, but the signal polarity is now reversed. Similarly, if $I_{b1} = I_{b2}$, there is exact cancellation of signal currents in the output without any change in the output common-mode voltage level. It can be seen that the relation between I_{b1} and I_{b2} determines the gain in continuous and linear manner according to:

$$G = G_{max}\left[1 - \frac{2I_{b2}}{I_{b1} + I_{b2}}\right]$$

The cascode configuration is inherently broad-band because the signal voltage swing at the collectors of the input devices (Q_1 and Q_2) is small. Any impedance in the collectors of these devices reduces the input impedance at high frequencies because it increases the voltage swing across the collector-to-base capacitance of the transistor. Thus, the absence of inductance in the collector leads of Q_1 and Q_2 is an inherent advantage of the integrated approach. The Gilbert multiplier of Fig. 1 retains the advantages of the cascode configuration independent of gain or polarity control.



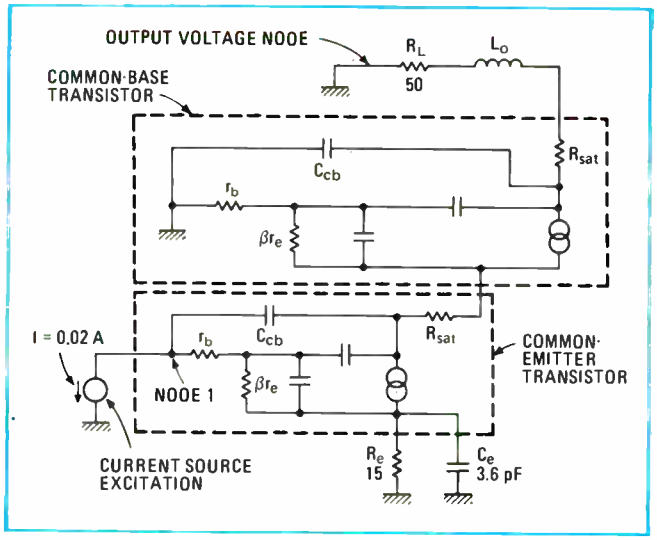
3. Peaking. Tee-coil interstage peaking circuit improves bandwidth by factor of 2.74 when driving R-C load. Bridging capacitance is chosen to make $Z_{in} = R_L$ at all frequencies.

Speeding up the transistors

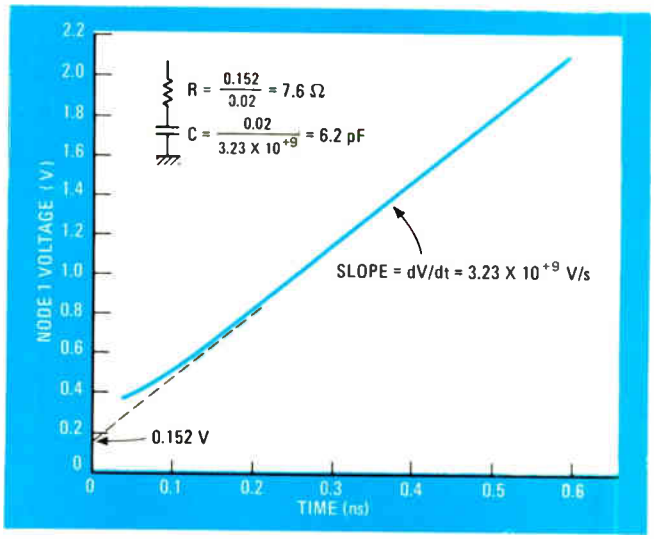
The transistors are biased at a current somewhat below their F_t peak and operate at only 2.4 volts collector-to-emitter to save power. Still, the F_t at this operating point is 3 gigahertz. To obtain this high F_t with low base resistance, the emitter width is held down to only 0.1 mil. Two base diffusions are used to maintain low base resistance without any sacrifice in beta or C_{eb}.

Integrated devices are slower than their discrete counterparts because of the large series resistance between the collector contact on top of the device and the collector region on the bottom. To reduce that resistance, a low-resistivity (deep collector) diffusion makes contact to a buried-layer collector.

To reduce capacitance between nearby devices, the isolation walls surrounding each collector region must be separated from each other. However, differential pairs of transistors must not be separated too far or temperature differences may result. While the small additional dc drift that this would cause is probably not significant, signal-related thermal effects are. Applying an input signal changes the power dissipated in Q_1 by an amount generally different from the power change in Q_2. This results in a temperature difference between Q_1 and Q_2 which is proportional to the input signal voltage (not the square of the voltage). The temperature difference changes the V_{BE} of both Q_1 and Q_2, giving rise to a new equivalent input signal. The effect is linear and not as small or as slow as one might expect—as much as 5% increase in gain at dc and a noticeable change in gain well above 1 megahertz.



4. Computer model. Model of cascode circuit is used in ECAP analysis of IC amplifier. L_o, inductance of the package's output lead, causes some overshoot in transient response (see Fig. 6).



5. Computer analysis. This is the calculated voltage response at node 1 of Fig. 4 to a 20-mA current-step input. For time frame of interest, input impedance looks like a series R-C circuit.

Actually, it is possible to bias a differential pair so that a condition called "thermal balance" prevails. At this point, defined by the equation

$$2I_sR_L = V_s + V_{BE} - (I_sR_E)/2,$$

there are no temperature-induced input signals. The equation is derived by setting the power-difference between Q_1 and Q_2 equal to zero for a non-zero differential signal input. In the equation, V_s is the collector supply voltage, I_s is the emitter supply current, R_E is the emitter gain-setting resistance, and R_L is the collector load resistance.

While most oscilloscope amplifiers are biased in this way, IC units usually cannot be made to satisfy the equation. Instead, they rely on close thermal coupling to keep the magnitude of the effects down to about 1% per stage, and the multiple time constants below about 10 ms—a manageable number. Nevertheless, between five and 10 compensation networks may still be required to flatten the remaining effects of thermal imbalance.

The ungrounded MOS capacitor

The MOS peaking capacitor is unlike many such integrated capacitors in that neither side is grounded. In both cases, the top plate is a large area of metal under which a thin layer of oxide serves as a dielectric. The bottom plate is the substrate, usually a negative power supply. Capacitors of 30 picofarads are quite commonly made in this fashion.

The configuration of Fig. 1 requires each plate to be connected to an emitter. Using two independent capacitors, one from each emitter to the substrate, is an unsatisfactory solution. The common-mode impedance at the emitter is lowered at high frequencies, and common-mode input signals couple through the substrate to the control bases. The common-mode gain is increased substantially and can easily exceed differential gain under these conditions. Oscillation is then possible in a multistage amplifier.

Fortunately, the buried-layer diffusion has low enough resistivity to serve as the bottom plate of a capacitor isolated from the substrate. The top plate and dielectric are the metal and underlying oxide as before. This materially reduces substrate excitation.

As might be expected, however, the buried layer has substantially more parasitic capacitance to the substrate than the metal, so that the emitter connected to that layer will also have greater capacitance to the substrate. Because of this imbalance, the substrate is now excited by differential as well as the remaining common-mode signals. The solution is to split the capacitor into two equal parallel capacitors. Each emitter is connected to one bottom plate and one top plate, preventing net substrate excitation. A photomicrograph of the chip and bonding is shown in Fig. 2.

To implement interstage inductive peaking, it is desirable to integrate only the emitter gain-setting resistor. However, since the gain actually depends upon the ratio of the gain-setting resistor to the load resistor, R_L, both resistors must have the same temperature coefficient of resistance. Since metal-film resistors are used for R_L, a diffused resistor, which has a temperature coefficient of about + 1,600 parts per million per degree centigrade, is an unsuitable choice for the gain-setting function.

Furthermore, it is important that the tolerance be good—especially in multistage amplifiers using the same chip repeatedly. A 10% gain error in each of five cascaded stages results in a 61% over-all gain error.

An excellent solution is to deposit a thin-film resistor directly onto the chip. Nichrome is used in preference to other metal systems, such as chromium silicides and tantalum, because the etchants usually used with these other systems are not compatible with silicon dioxide or aluminum. Additionally, it has a temperature coefficient of resistance of less than 100 ppm/°C and can be made with the low sheet resistivity (10 ohms/square) required for an emitter resistor of only 30 ohms.

Large bandwidth and smooth frequency response depend heavily upon a good system of interstage peaking. One of the best of such systems is the tee-coil circuit (Fig. 3), in which the tee-coil is actually a pair of mutually coupled inductances. The use of a tee-coil to con-

nect an RC load to a source, such as the output of one stage of a multi-stage amplifier, improves the bandwidth by a factor of 2.74 while adding only 0.4% of overshoot. The 3-dB bandwidth of a tee-coil peaked amplifier is given by $\Delta f = 2.74/2\pi(R_L + R_{in})C_{in}$, where the circuit is assumed to be tuned for a maximally flat envelope delay response.

Adding C_b, the bridging capacitor, transforms the circuit into a "bridged tee-coil" and gives it another extremely useful property: if $C_b = (C_{in}/12)[(R_L + R_{in})/R_L)]^2$, then the driving-point impedance, Z_{in}, is real and equal to R_L at all frequencies.[2]

Having a constant, real, driving-point impedance makes it possible to use etched-circuit-board transmission lines for interstage coupling, without any need for reverse terminations—that is, no collector loads are required in the driving stage. In principle, one could doubly terminate an interstage transmission line of twice the impedance and use simple inductive peaking at each end without any loss of gain or bandwidth. However, the tee-coil does a better job of preventing signal reflections between stages.

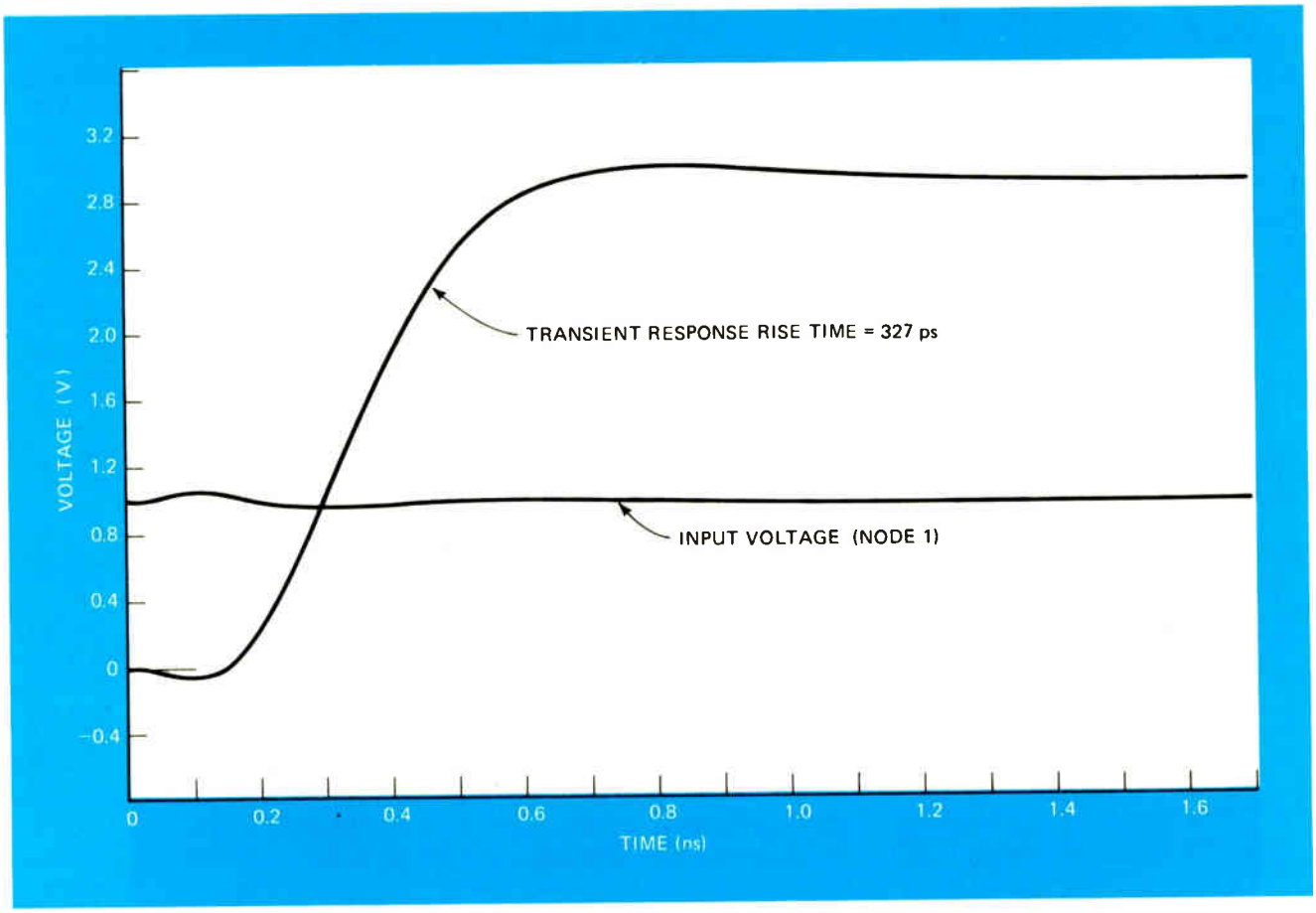
Before implementing tee-coil peaking, one must know accurately the input impedance of the stage to be peaked. This may entail considerable work by any method, but the method used here—computer analysis based on a well-tested transistor model—is fast and intuitively appealing. The analysis is carried out with IBM's well-known electronic circuit analysis program (ECAP) using the circuit model of Fig. 4. The value of R_e is derived from a dc analysis of the required gain. C_e is given by $C_e = 1/2\pi F_t R_e$.

A mathematical time-domain reflectometry analysis is performed with the computer; a 20-milliampere current-step input excitation is programed, and the voltage at node 1 (Fig. 5) is observed.

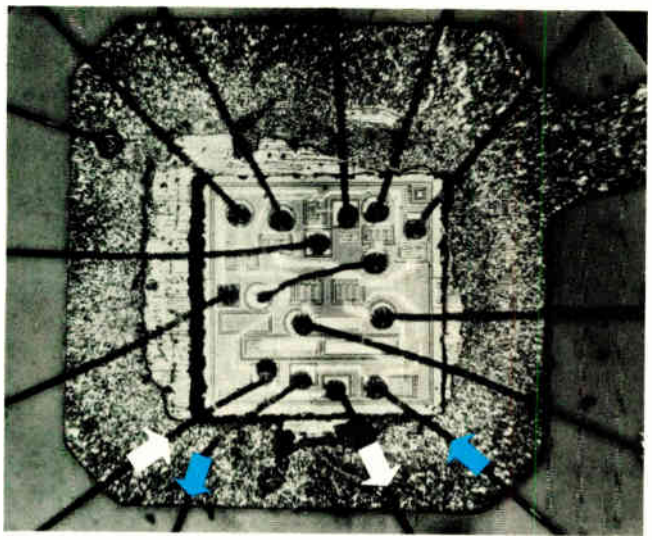
Since the voltage starts out at 0.152 volt, it is clear that the input at $t=0$ looks like a resistance of value $R = 0.152\ V/20\ mA = 7.6$ ohms. The constant slope of $dV/dt = 3.23 \times 10^9 V/second$, for values of t greater than 0, corresponds to a series capacitance of $C = 20\ mA/3.23 \times 10^9\ V/s = 6.2\ pF$. Thus the input impedance looks like a simple series RC circuit.

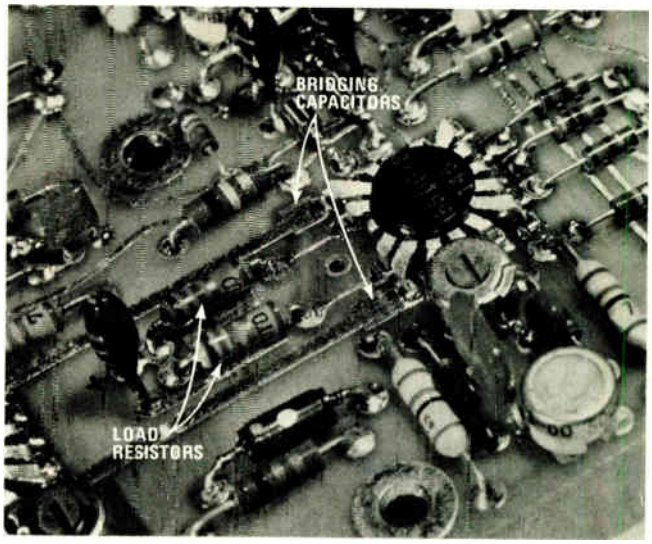
Simple theory which neglects the Miller effect and R_{sat} predicts that C_{cb} is in parallel with the series combination of r_b and C_e. Actually, the Miller effect operates on r_b and C_{cb} to reduce the resistive component below r_b and to raise the capacitive component to a value greater than $C_{cb} + C_e$. The surprising fact remains that, within the time of interest (the amplifier risetime), a single series combination of resistance and capacitance adequately describes the circuit input impedance.

The proper tee-coil is then designed and interposed between the current source and the amplifier input. Another computer TDR analysis and, this time, a transient-response calculation, as well, are performed as a check. The overshoot in the transient response (Fig. 6) is caused by the package lead inductance at the output (L_o



6. Double check. Again the computer calculates amplifier's response to a current step input, but this time with a tee-coil between the current source and the amplifier. In addition to the node 1 input voltage, the amplifier's output is plotted.





7. A chip trick. Tee-coil is realized by looping the input signals through the IC package as indicated by arrows on photograph of the chip. Small run of metal between load resistors and the IC adds extra inductance required by the output leads. Top plates of the bridging capacitors are seen as large square metalization areas at the corner input pins of the IC package.

in Fig. 4). It is interesting to note that the risetime is within a few percent of the value predicted from consideration of the tee-coil alone. This means that only the input impedance limits the bandwidth and that interstage peaking is very important.

To make use of the package lead inductance, the input signal is "looped through" the package. Each of the push-pull inputs enters a corner pin, leaves one of the inner pins on the same edge, and terminates in a 50-ohm load resistor, R_L. Fortunately the value of L_1, the tee-coil input inductance, is just that contained in the corner pin of the IC package (Fig. 7). The adjacent pin has slightly less inductance than required for L_2, and additional inductance is obtained with a narrow etched-circuit-board run between the pin and the load resistor.

The bridging capacitance, C_b, is obtained by using a three-layer etched-circuit-board capacitor, the top plate of which may be seen as a wide area next to the corner package pin in the photograph of the etched-circuit-board in Fig. 7. The required 0.68 pF is obtained with just 0.01 square inch of board area.

A cool package

A new inexpensive epoxy package design was chosen for the IC. Because the leads are both short and roughly equal in length, power dissipation exceeds that of a 16-pin dual-in-line package and is rated at 400 milliwatts. The IC actually dissipates less than 150 mW typically and therefore runs very cool. The package may be plugged into the circuit board for easy removal. □

REFERENCES

1. Barrie Gilbert, "A New Wide-Band Amplifier Technique," IEEE Journal of Solid State Circuits, Vol. SC-3, No. 4, December 1968, p.353.
2. Robert I. Ross, unpublished Tektronix paper, Feb. 19, 1969.

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The first practical application

The first commercial use of the new integrated circuit is in Tektronix's Type 485 350-megahertz portable oscilloscope. A total of 17 of the ICs is used—eight in the vertical and internal trigger amplifiers, two in the main vertical amplifier, six in the A and B trigger amplifiers, and one in the A external trigger display. The high gain-bandwidth product of the IC is largely responsible for the scope's 5-millivolt sensitivity at 350 MHz. The oscilloscope's input impedance can be switched from 1 megohm to 50 ohms at the touch of a front-panel button.

The entire unit weighs just 20½ pounds without accessories. This extremely light weight is traceable, at least partially, to the new IC, because it keeps the scope's power consumption to a mere 60 watts overall. Low power consumption requires only a small, lightweight power supply, which means that heavy cast parts are not needed for structural strength.